STREAMLINED INTERCONNECTION ANALYSIS OF DISTRIBUTED PV USING ADVANCED SIMULATION METHODS

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STREAMLINED INTERCONNECTION ANALYSIS OF DISTRIBUTED PV USING ADVANCED SIMULATION METHODS

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NOMENCLATURE

AI	Allowed Interconnections
AM	Air Mass
ANN	Artificial Neural Network
ANSI	American National Standards Institute
CBEMA	Computer Business Equipment Manufacturers Association
CDF	Cumulative Distribution Function
CLASS	Comprehensive Large Array-Data Stewardship System
COM	Component Object Model
CSI	Clear Sky Irradiance
CVR	Conservation Voltage Reduction
DG	Distributed Generation
EPRI	Electric Power Research Institute
FERC	Federal Energy Regulatory Commission
FIRST	Feeder Impact Risk Score Technique
GHI	Global Horizontal Irradiance
GIS	Geographic Information System
GOES	Geostationary Operational Environmental Satellite
GridPV	Grid Integrated Distributed PV
GSIP	GOES Surface and Insolation Products
GUI	Graphical User Interface
HC	Hosting Capacity
IST	Interconnection Screening Threshold

ITIC	Information Technology Industry Council
LDC	Load Drop Compensation
LHC	Locational Hosting Capacity
LTC	Load Tap Changer
MIDC	Measurement and Instrumentation Data Center
MV	Medium Voltage
NN	Neural Network
NOAA	National Oceanic and Atmospheric Administration
NREL	National Renewable Energy Laboratory
OLTC	On-load Tap Changer
OpenDSS	Open Distribution System Simulator
PAI	Potentially Allowable Interconnections
PCC	Point of Common Coupling
PF	Power Factor
PPI	Potential Percent Increase
pu	Per unit
PV	Photovoltaic
QSTS	Quasi-static Time-series
SAR	Screen Accuracy Ratio
SCADA	Supervisory Control and Data Acquisition
SGIP	Small Generator Interconnection Procedure
SoDA	Solar Radiation Database
TMY	Typical Meteorological Year
TOV	Temporary Over-Voltage
UNLV	University of Nevada, Las Vegas

VI	Variability Index
VREG	Voltage Regulator
VSA	Violation the Screen Allowed
WECC	Western Electricity Coordinating Council
WVM	Wavelet Variability Model

SUMMARY

With the penetration of PV on the distribution system continually increasing, new advanced simulation methods are necessary to model the potential technical impacts of PV to the equipment and operation of the distribution system. Conventional analysis of the distribution system could historically be performed for a single period at the peak load time and only had to consider power flowing in a single direction. With distributed PV, a timeseries analysis approach is necessary to more fully capture the time-varying nature of solar energy and the interaction with distribution system operations. The objective of the research is to streamline the PV interconnection process by providing more accurate methods that require less time for both the PV interconnection screening criteria and the PV interconnection impact study process. For the continued advancement of solar energy, the modeling accuracy is crucial to correctly and easily allow interconnections that will not cause issues, while at the same time not installing systems that will require costly upgrades in the future because the issues were not detected before the system was installed. The impact of different variability profiles, regulator control algorithms, and smart inverters with volt/var functionality are all demonstrated in quasi-static time-series (QSTS) simulations.

Due to the large number of PV interconnection requests, distribution system modelling must also be accomplished quickly. To improve the computational speed of timeseries simulations, an equivalent circuit reduction method is developed to simplify the circuit to a reduced-order model. The reduced circuit is equivalent during timeseries simulations, but it solves in a fraction of the time. The algorithm works with unbalanced multi-phase complex distribution system models, and it is shown to have high accuracy when validated against the full feeder models.

An advanced PV hosting capacity simulation tool is developed and used to quantify system impacts for many PV interconnection scenarios, configurations, and

locations, which can be generalized to develop improved future interconnection screening criteria. The advanced tools quantify location-specific impacts and the locational hosting capacity of potential PV interconnection locations on the feeder, including PV impact signatures and zones. A set of 50 different real distribution systems is analyzed in detail to demonstrate the range of scenarios and impacts that can occur depending on the feeder characteristics and topology.

Specific methods are developed for time-series analysis, faster simulation times, distribution system equivalent circuit reduction, and PV hosting capacity analysis. The advancements presented in this thesis assist in streamlining PV interconnection studies with faster interconnection analysis times and more accurate screening criteria.

CHAPTER 1: INTRODUCTION

1.1 Problem Statement

Deployment of distributed PV systems is increasing rapidly. High penetration scenarios, which are becoming increasingly common, have the potential to affect the distribution feeder equipment [1] and the operation of the distribution system in general. Interconnection study processes are developed to identify possible system impacts and, in the case of negative impacts, design mitigation alternatives [2]. In the majority of cases, system impacts can be ruled out or mitigation strategies can be identified without an involved study by using a screening process or a simple supplemental review study [3]. For proposed projects that require a closer evaluation, the existing methods, data, and simulation tools may not be adequate to fully characterize the potential system impacts. Enhanced system impact studies are required to identify the potential electrical impacts associated with the integration of PV on the distribution system [4, 5].

Existing screening criteria, such as the 15% of peak feeder load screen, have provided an easy threshold method for the initial screening of PV interconnections, but there is room for improvement in quickly detecting which PV systems will not have significant impacts. If an interconnect does not pass the screening criteria, the detailed PV interconnection impact study can be time consuming and a slow process to analyze all potential impacts. The prospect of high penetration scenarios requires improvements in analysis methods and simulation tools.

1.2 Research Objectives

The objective of the research is to streamline the PV interconnection process by developing advanced simulation methods for analyzing and determining any potential electrical impacts of high penetrations of PV on the distribution system. The scope of the

work is limited to the technical impacts of PV on distribution system operation, which is separate from any transmission impacts, economic or market impacts, and environmental factors. The research focuses on both the PV interconnection screening criteria and the PV interconnection impact study process. The goal is to provide more accurate methods that require less time. To accomplish this, new tools, methods, and algorithms are created for detailed analysis of PV variability in time-series simulations. This research focuses on the methodology for interconnection studies, the tools necessary to perform interconnection studies, different placement scenarios for distributed solar, and the difference in impacts caused by the specific location of the interconnection on the distribution system.

The interconnection study process can be streamlined by developing a method for simplifying the complex system to an equivalent representation of the feeder. A full detailed model of the distribution system can be time consuming to produce and requires more computational effort to run in simulations. A simplified equivalent circuit retains the general characteristics of the distribution system while providing reduced modeling effort. The objective of this feeder simplification research is to take a distribution feeder, which will typically have hundreds of line sections and nodes, and to reduce it to an equivalent circuit with far fewer line sections and nodes where only a couple inputs are needed to test all interconnection criteria.

Finally, novel methods are developed for analyzing PV interconnections with advanced simulation methods using location-specific impacts and locational hosting capacity of PV interconnections. An advanced simulation tool is developed to quantify system impacts for many PV interconnection scenarios, configurations, and locations. This new tool generates feeder PV impact signatures by running a large combination of different PV deployment scenarios. The hosting capacity analysis is performed on a range of different distribution systems to understand the risks associated with interconnecting PV on different feeder topologies.

Specific methods are developed for time-series analysis, faster simulation times, distribution system equivalent circuit reduction, and PV hosting capacity analysis. The advancements presented in this thesis assist in streamlining PV interconnection studies with faster interconnection analysis times and more accurate screening criteria.

1.3 Outline of Chapters

In Chapter 2, an extensive review of modeling the technical impacts of PV on the distribution system is provided. Special attention is given to modeling the solar irradiance variability, which provides a crucial input to performing timeseries analysis. The chapter also includes a literature survey of the traditional methods of modeling PV, a summary of the typical interconnection process, and an overview of the potential impacts that PV can have on distribution system operations. Previous circuit reduction methods are also reviewed.

In Chapter 3, a timeseries approach for modeling PV impacts is presented. The motivation for quasi-static time-series (QSTS) is shown by looking at the variability of PV and the interaction with the distribution system. Extreme voltage, both high and low, can only be captured when modeling the time-varying nature of PV and load. Solar variability also interacts with voltage regulation equipment to increase the number of tap changes. This interaction is studied in detail for various PV variability profiles, simulation parameters, and voltage regulator control settings. Finally, improved computational methods are demonstrated for increasing the speed of QSTS analyses.

In Chapter 4, a circuit reduction method is developed in order to reduce very large complex distribution system models to a simpler, yet equivalent, system. The algorithm is initially developed for balanced 3-phase systems in order to prove the equivalence of the algorithm. The methodology is expanded to be applied on more realistic distribution systems with unbalance, mutual line impedances, line charging capacitance, and transformers with core losses. The algorithm is implemented in MATLAB and applied to

large distribution systems with thousands of buses. The circuit reduction is shown to work for several different feeders, with high accuracy when validated against the full models.

In Chapter 5, advanced simulation methods for PV interconnection analysis are presented. An advanced simulation tool is developed to quantify location-specific impacts and the locational hosting capacity of potential PV interconnection locations on the feeder. The locational analysis is expanded to analyze entire feeders with PV impact signatures and zones. Finally, a set of 50 different real distribution systems is analyzed in detail to demonstrate the range of scenarios and impacts that can occur depending on the feeder characteristics and topology.

In Chapter 6, a summary of the key results and conclusions of the research are presented. Contributions of the research are included, along with potential future research directions.

CHAPTER 2: LITERATURE SURVEY AND RESEARCH CONTEXT

2.1 Introduction

This chapter provides a literature review of the electrical impacts that PV can have on the distribution system and the methods currently used to analyze PV interconnections for potential issues. The second part of the chapter discusses existing techniques for reducing electrical grid models into simpler representations.

2.2 Modeling Solar Generation Inputs for Interconnection Studies

A critical input for simulating the impact of PV interconnections on the distribution system is the modeling of the solar resource and PV power production. This section largely focuses on modeling the expected solar irradiance for generating power output timeseries and total PV energy produced. The irradiance profile is first converted to plane of array irradiance [6], smoothed according to PV plant size [7] and wind speed [8], and then converted to expected AC power output using PV array [9] and inverter [10] performance models.

2.2.1 Clear Sky Models

Often distribution planners are most interested in the largest impact that PV could have grid. This happens on clear days when the highest solar energy is produced, therefore many grid impacts can be studies solely using the diurnal solar patterns of the expected irradiance. This type of analysis will often over estimate certain impacts, such as yearly losses, but because it does not account for solar variability, it will under-estimate other potential impacts like flicker or voltage regulator tap changes. Clear sky irradiance profiles provide a solid starting foundation for modeling grid impacts.

Clear sky models estimate the terrestrial solar radiation under a cloudless sky as a function of the solar elevation angle, site altitude, aerosol concentration, water vapor, and various atmospheric conditions [11, 12]. Global horizontal irradiance (GHI) clear sky models vary from very simple to complex [13]. There are also many published clear sky models that can be applied for different latitudes, longitudes, and elevations. Some very simple models that only depend on solar zenith angle include Daneshyar–Paltridge–Proctor model [14, 15], Kasten-Czeplak [16], Haurwitz [17, 18], Berger–Duffie [11], and Robledo-Soler [19]. Some simple models that include one or two additional parameters are Kasten model [20] and Ineichen model [21]. Complex models, such as MAC [22, 23], Atwater and Ball [24, 25], Bird [26, 27], and REST models [28-31], are highly accurate when all of the inputs are correctly measured. Validation of clear-sky models requires comparison of model results to measured irradiance during clear-sky periods and is performed for selected clear-sky models using measured data from 30 different sites in [13]. In terms of error averaged over all locations and times, [13] found that complex models that correctly account for all the atmospheric parameters are slightly more accurate than other models, but, primarily at low elevations, comparable accuracy can be obtained from some simpler models. Other authors have also found that simple models are comparable in accuracy to more complicated models [11]. The development of a complex clear sky model for a location is a time consuming processing, and complex models are also heavily dependent on having local measurements [32].

2.2.2 Solar Irradiance Variability

Because of location-specific weather and cloud cover, the irradiance at a given place on earth does not match the clear sky models previously mentioned. Using historical measurements or satellite data, the actual average irradiance can be found for each day of the year. Two good sources of data are Typical Meteorological Year (TMY) [33] or satellite data [34]. Both of these provide a profile more characteristic of the

irradiance for a location's given weather patterns. This data can be used to calculate how much solar energy will be produced throughout the year and to perform other high-level yearly simulations.

For distribution system assessment of solar PV impacts, the common concern is intermittency and variability of solar energy and how this might impact nearby customers on the distribution system. These issues all relate to the frequency and speed for which the PV output will change. High time-resolution irradiance data is required for this type of analysis.

One method to determine the amount of solar variability is by the type of cloud. Innately, solar variability is caused by cloud cover, so depending on the structure, speed, and opacity of the cloud, the PV output variability will change. If the cloud type is known, or forecasted, control algorithms for energy storage, spinning reserve, or optimal dispatch could be controlled based on the expected variability and ramp rates from solar power plants for that period. It could also be used to model the solar variability for a given location and time by synthetically creating time series irradiance data. The frequency of each cloud category could be used to distinguish the differences in variability for different locations and regions.

Imagery from GOES satellites is analyzed to determine how solar variability is related to the NOAA classification of cloud type [35]. Without using a model to convert satellite imagery to average insolation on the ground, cloud categories can directly model the expected statistical variability of ground irradiance. Classifying the types and properties of each cloud class is an interesting research problem that historically was done by trained human observers. With satellite images and data, clouds and weather patterns can be classified for large geographic areas. From the ground, sensors such as irradiance sensors can categorize cloud cover or cameras with image processing can detect and recognize types of clouds. Tapakis and Charalambides provide a detailed overview of all methods for detecting and classifying clouds using the full variety of

sensors and cameras on the ground or in space [36]. Duchon and O'Malley defined a cloud classification method using time series data from a pyranometer to categorize clouds into one of seven types with a 21 minute running mean and standard deviation of irradiance [37]. In [38], this method was found to be usable for classifying the clouds in Antarctica, and more detailed and accurate criteria were proposed. Another method proposed using time series global and diffuse irradiance data and five different statistical metrics to cluster the time series data into several classes and determine the number of oktas with cloud cover [39]. In South Dakota, a four band (440 to 936 nm) photometer measured shape was fit into one of nine cloud types using a decision tree [40]. Finally, a method was developed to classify clouds with combinations of attenuations in the beam transmittance and visual identification from sky images [41].

Image processing can provide autonomous classification of clouds from images taken from the ground at regular intervals. In [42], sky photographs were used to create cloud contours with fractals, synthesize cloud patterns, and create time series irradiance data. A whole sky imaging system was used in [43] and [44] to classify cloud types in the image based on color and texture. The spatial cloud variability can be used to classify clouds into five different classes, where each cloud class relates to a irradiance variability class [45]. The irradiance variability class allows an irradiance time series to be synthetically created that statistically represents the expected measured irradiance on the ground.

The GOES Surface and Insolation Products (GSIP) created by NOAA from process GOES satellite data also includes cloud type [46]. GOES West hourly GSIP images were downloaded from April 2009 to July 2011, totaling ~350 GB of data. The satellite images are compared to global horizontal irradiance at two NREL MIDC locations during the same time period [47]. UNLV is the University of Nevada, Las Vegas, and Anatolia is in Rancho Cordova, California. The irradiance is converted to a clear sky index using a clear sky model that provides a much more accurate

representation of the expected shape for clear sky irradiance on the ground [13, 48]. The clear sky model used is the Ineichen model [21]. The inputs to this model are solar zenith (z), air mass (AM), Linke Turbidity (TL), and elevation (*h*). Kasten and Young's formula is used to calculate the air mass [49]. Remund calculated and produced Linke turbidity maps for the world for each month using a combination of ground measurement and satellite data [50] that can be downloaded from either the HelioClim website [51] or Solar Radiation Data (SoDa) website [52].

With hourly images, a 40 km square is used to represent the irradiance time series information for the 30 minutes before and after the image is taken. The cropped satellite image is processed for the mean cloud type, largest number cloud type, smallest number cloud type, and the range of cloud types in the 16 pixels. The cloud type and corresponding number are shown in Figure 1. These cloud statistics are analyzed and compared to the 60 minute clear sky index time series around the image snapshot.

The type of cloud impacts the percentage of sunlight transmitted through the cloud. To analyze this, the average clear sky index is calculated for each daylight hour and is plotted in Figure 1 compared to the mean cloud type for Anatolia. Note that the order has been changed with type 5 (optically thin ice cloud) plotted between type 2 (water cloud) and type 3 (supercooled cloud) instead of with the optically thick clouds (type 4). A clear trend and average clear sky index can be associated with cloud type, although there is considerable scatter.

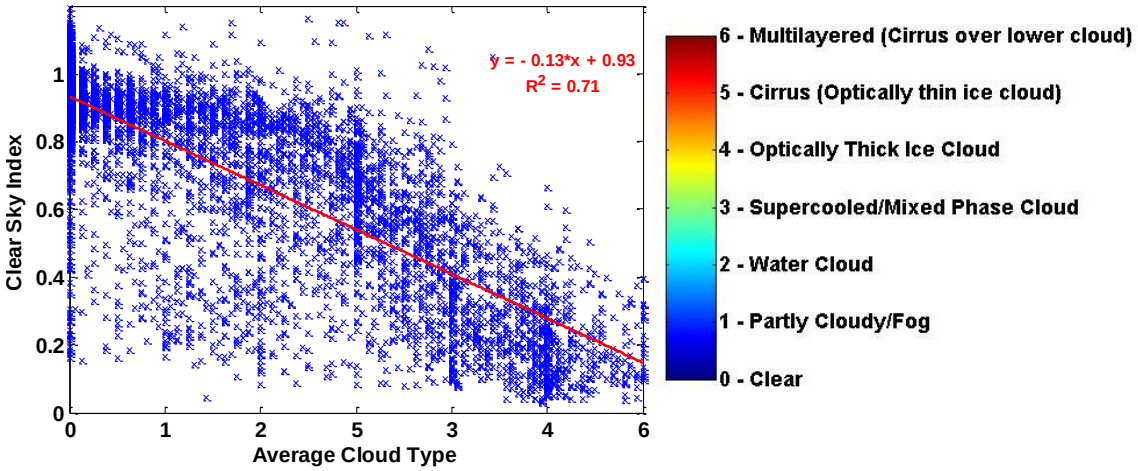


Figure 1. Measured clear sky index at Anatolia compared to GSIP cloud categories during all daylight hours.

The distribution of clear sky index for each cloud type is shown in Figure 2. In [53], the frequency distribution of clear sky index is listed at the first criteria for characterizing irradiance time series, and the second criteria considering ramp rates is discussed later. The mean clear sky index for the cloud type is shown with a vertical red line, and both the numeric values for the mean and mode clear sky index are noted on the plots.

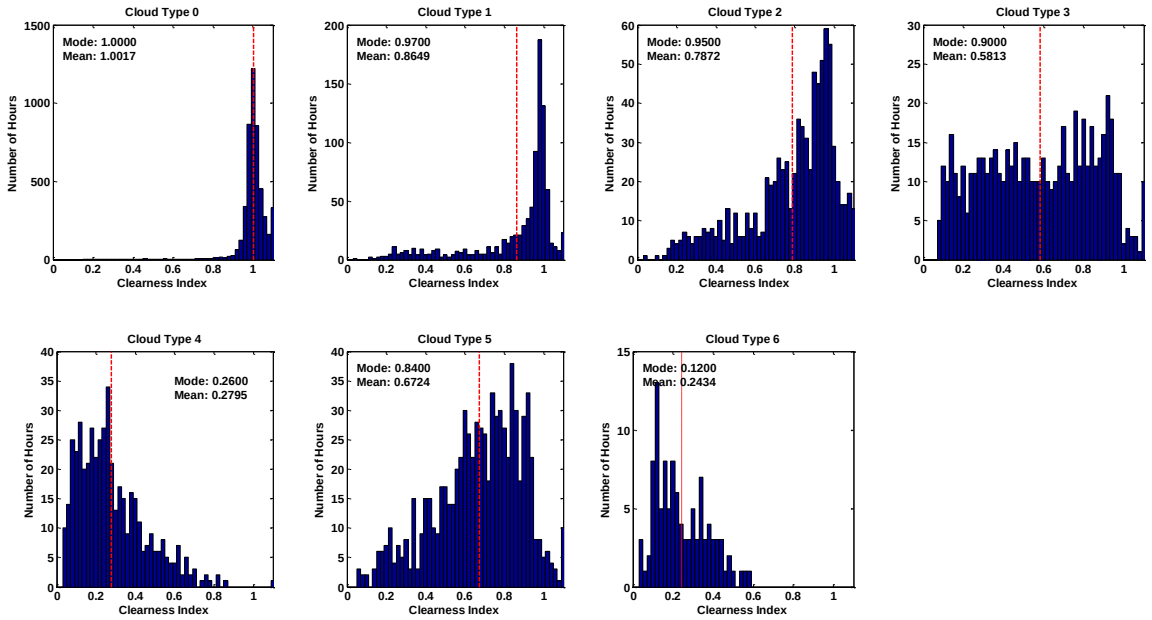


Figure 2. Measured clear sky index at Anatolia compared to GSIP cloud categories

The average clear sky index was shown to be dependent on the cloud type, and the variability is also influenced by the cloud category. Irradiance variability can be defined and calculated many different ways, but the easiest method is to calculate the standard deviation of the time series data. Similar to [37], the mean and standard deviation of clear sky index for the period 30 minutes on either side of the image are plotted in Figure 3. This illustrates that types of clouds are generally in certain regions of the graph with specific clear sky indices and variability.

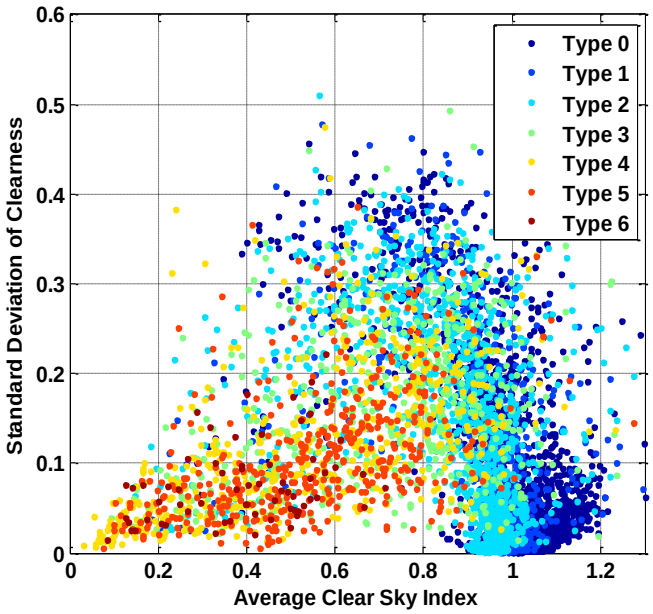


Figure 3. Mean and standard deviation for the 1-hour clear sky index time series around the cloud type image for daylight hours at UNLV.

A metric for measuring variability called Variability Index (VI) was proposed in [54]. For the hour around the image, VI is calculated as:

$$VI = \frac{\sum_{k=2}^{n} \sqrt{(GHI_k - GHI_{k-1})^2 + \Delta t^2}}{\sum_{k=2}^{n} \sqrt{(CSI_k - CSI_{k-1})^2 + \Delta t^2}} \qquad (1)$$

where *GHI* is a vector of length *n* of global horizontal irradiance values measured at some time interval in minutes, Δt. *CSI* is a vector of calculated clear sky horizontal irradiance for the same times as the *GHI* data. The average VI for each cloud type is

shown in Figure 4. Note that the shape of the variability by cloud type is very similar between the two locations. If there is Type 2 cloud without Type 0 or Type 1, VI is high. It can also be noted that Type 4 in generally has lower variability.

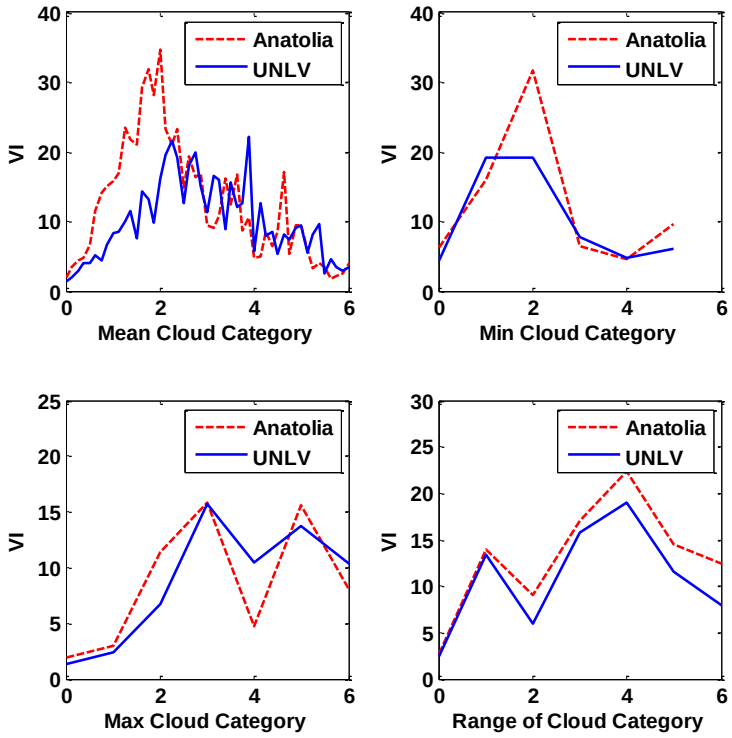


Figure 4. Average VI by cloud type for each daylight hour at UNLV and Anatolia.

Another method to characterize irradiance variability is to measure the magnitude of the ramp rates. The magnitude and frequency of the irradiance time series variability was previously discussed using VI and standard deviations, and the rate of the increase and decrease of irradiance is characterized using the ramp rate. Ramp rates are often compared between sites, different time scales, or between irradiance and power output, but our study compares ramp rates for different cloud categories. The 1-minute ramp rate is calculated as the absolute value of the difference between the clear sky index at each minute. The cumulative distribution function (CDF) for the 1-minute ramp rates during each cloud type are shown in Figure 5 for Anatolia and UNVL from April 2009 to July 2011. The first graph is grouped by the mean cloud type in the 4x4 pixel satellite image, and the second row is grouped by the largest cloud number in the window. Even with the

limited analysis dataset, it appears to be fairly consistent as to which clouds have higher ramp rates, independent of location. For example, a ramp rate of >0.4/minute for a mean cloud type of Type 2 (1.5% of the time at UNLV, and 3% of the time at Anatolia) is around 10 times more likely than if the mean cloud type is Type 0 or Type 5 (0.15% of the time at UNLV, and 0.3% of the time at Anatolia). Looking at the maximum cloud type, a ramp rate of >0.4/minute for a maximum cloud type of Type 3 (2% of the time) is 4 times more likely than if the maximum cloud type is Type 4 or Type 6 (0.5% of the time). If the ramp rates can be precisely correlated to cloud type, the expected distribution of ramp rates for a location can be determined by the distribution of cloud types in historical satellite imagery.

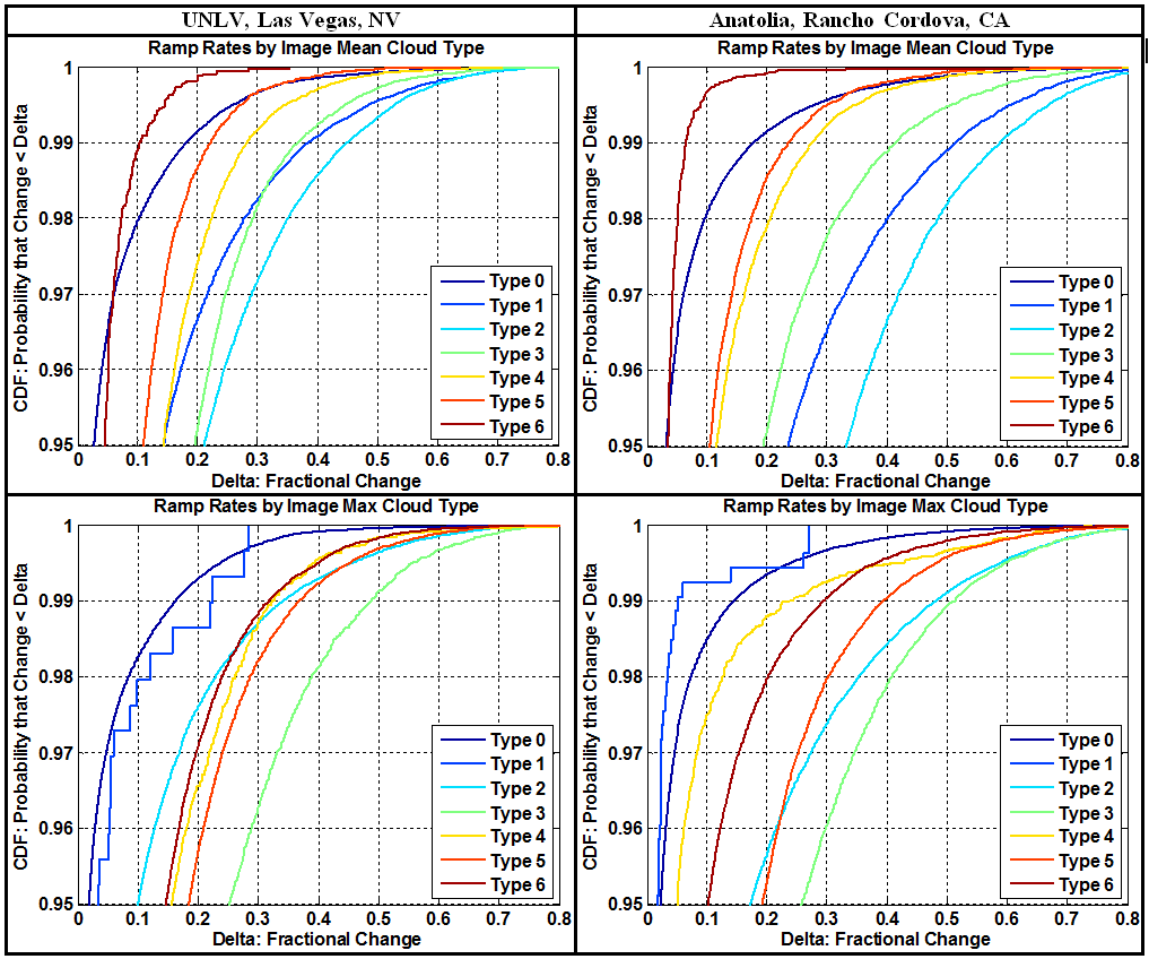


Figure 5. CDF of the 1-minute ramp rates for two locations by cloud type.

The NOAA classification of cloud type is useful for characterizing the irradiance during the time period. Hourly cloud classified satellite images are compared to multiple years of ground measured irradiance at several locations to determine if measured irradiance, ramp rates, and variability index are correlated with cloud category. It was shown that the mean value and distribution of ground irradiance, the variability, and the distribution of ramp rates are dependent on the cloud category. Using this method to model irradiance and variability from cloud type, satellite imagery and the prevalence of each cloud type at a location can be used to produce synthetic time series irradiance or represent the long-term irradiance distribution and variability profile for the location.

2.2.3 Solar Modeling Using Satellite Imagers

Using satellite imagery to identify cloud types and patterns can predict irradiance variability in areas lacking sensors. With satellite imagery covering the entire U.S., this allows for more accurate integration planning and power flow modeling over wide areas. Satellite imagery of southern Nevada is analyzed and methods for image stabilization, cloud detection, and textural classification of clouds are developed and tested in [55]. The purpose in [55] is to translate satellite imagery into a model of irradiance, variability, and PV output for a fleet of PV plants at one minute resolution that can be easily implemented into a power flow model of the area. Current techniques of estimating high frequency (<1hr) solar resource data generally rely on direct measurements of irradiance. Being able to estimate high frequency irradiance (~1 min) from satellite imagery allows the grid impacts of distributed and utility-scale solar generation to be evaluated. Utilities and energy planners need to know how solar photovoltaic plants will affect the operation of the grid in order for these plants to be built, and high frequency solar resource data is needed as input for these studies.

The satellite imagery used is from the Geostationary Operational Environmental Satellite (GOES) which is owned and operated by NOAA through their Comprehensive

Large Array-Data Stewardship System (CLASS). The proposed method uses GOES West or GOES-11 which is located at longitude 135.0W at 35,790 km above the equator and has been in operation since 6/21/2006. The visible wavelength (0.55 to 0.75 Âµm) silicon detector is used for images with 1 sq-km per pixel resolution taken approximately every 15 minutes [46].

There are several groups that have developed algorithms to model average ground irradiance using satellite imagery [56, 57] that have been shown to be highly accurate [58]. The model in [55] is verified with one minute irradiance and power output data provided by Las Vegas Valley Water District (LVVWD) from six of their PV plant sites in the Las Vegas area starting in August 2006. The NREL Measurement and Instrumentation Data Center (MIDC) also provides one minute irradiance data for two sites in the area starting in March 2006 at Clark Station and the University of Nevada. In Figure 6, an example GOES images around 4:00PM (PST) on June 4, 2008, shows the correspondence with the ground irradiance measurements at two ground locations, Fort Apache and UNLV.

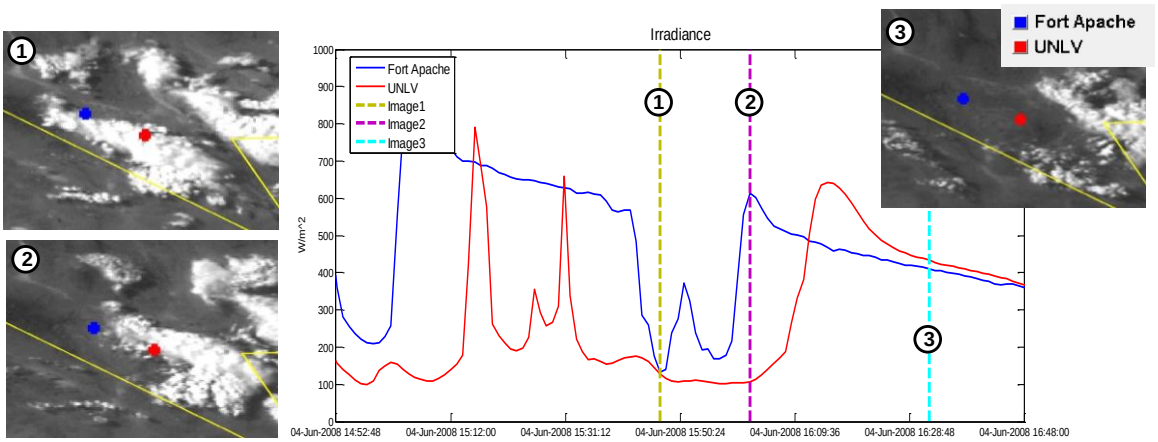


Figure 6. Three images from GOES 11 of Las Vegas region for 6/4/2008 around 4PM (PST) with corresponding measured irradiance at two ground locations.

The model in [55] for converting satellite imagery to high-resolution irradiance data is shown in Figure 7. The irradiance is modeled at one minute resolution between two historical satellite images 15 minutes apart. First, the images go through image

processing such as geographical subsetting, image stabilization, and cloud detection. The processed images have the background image of the ground on a clear day subtracted out to leave only the clouds in the image. The two images are translated into clearness indexes through the trained artificial neural network (ANN) model. The ANN was trained using images and known historical 1-minute clearness indexes from measured irradiance data. Finally, the clearness index is transformed back to irradiance measurements using the clear sky model.

The image processing and background subtraction are described in more detail in [55], and the main solar variability modeling is accomplished using an ANN to learn the correlation between identified clouds and the high-resolution solar variability for the time period between the images. This is a type of artificial learning to automatically categorize and cluster cloud types and the matching types of variability. Training was done with multiple ground locations with thousands of satellite images throughout the year.

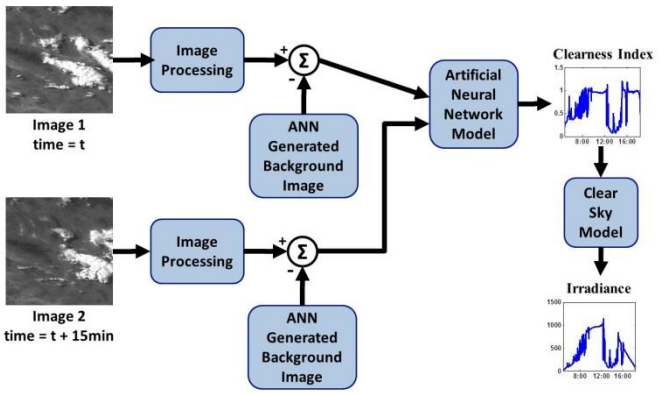


Figure 7. Model overview using two images 15 minutes apart to generate the irradiance profile for each minute between images.

In order for the neural networks to learn the correlation between the clouds and the ground irradiance, the background image of the ground must be removed. Background subtraction was accomplished in [55] by estimating what an image of the ground would look like and subtracting this image from the actual image. As a result of background subtraction, the subsequent image analysis depends only on the clouds in the

image, and not on any of the background content. An additional ANN can be used to generate the background image that varies with the seasonal and daily changes. This ANN is automatically trained by detecting and using only images of the location without clouds throughout the year. For each of the images with clear skies, image statistics (mean, minimum and maximum) of the pixel intensity are computed. It can then generate what an image would look like for any date for that location without clouds. The synthetic background images are verified to match the min, max, and mean intensity for each time and day of the year.

The background image generation is validated in Figure 8a, which shows the neural network was found to produce synthetic images which had statistics reasonably close to the statistics for the actual clear day images. Figure 8a shows that the synthetic image retains the general structure and characteristics evident in the GOES-11 image. Figure 8b shows that the ANN also learned the diurnal variation through the year to account for different lengths of days and solar intensity.

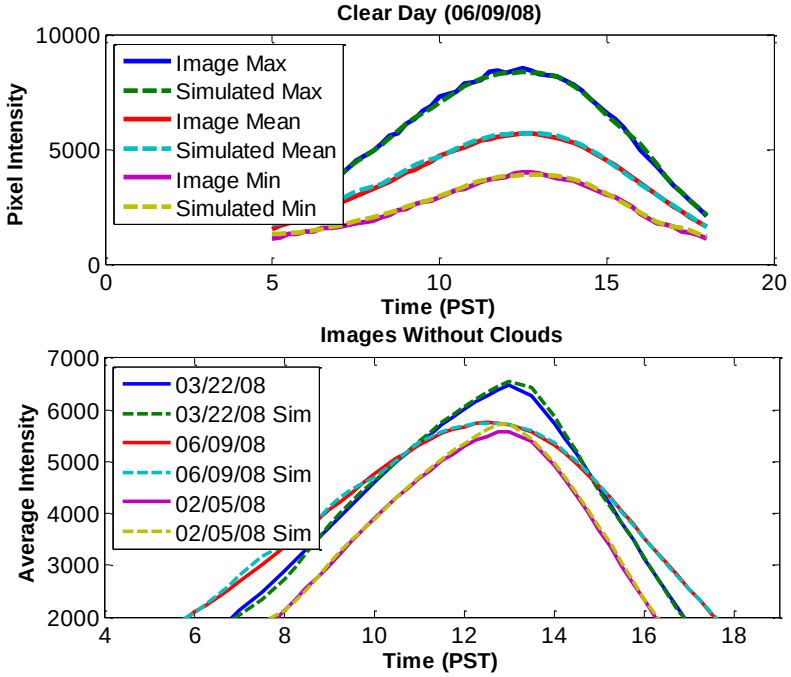


Figure 8. Comparison of pixel intensity of clear sky images and ANN simulated output for a) Diurnal variation in image statistics and b) diurnal variation for different days of the year.

The ANN model was trained using measured ground irradiance between the two images 15 minutes apart. The irradiance was transformed to clearness index by dividing by the clear sky model irradiance. The feed-forward back-propagation ANN was set up with three hidden layers of 300 neurons with a log-sigmoid transfer function. The BFGS quasi-Newton backpropagation algorithm in MATLAB was used to train the ANN with the satellite images as inputs and the ground clearness index as the output. One week of images and data was used the train the ANN model. An example of the model learning the training data is shown in Figure 9 where the model learned the correlation between the images and irradiance very accurately.

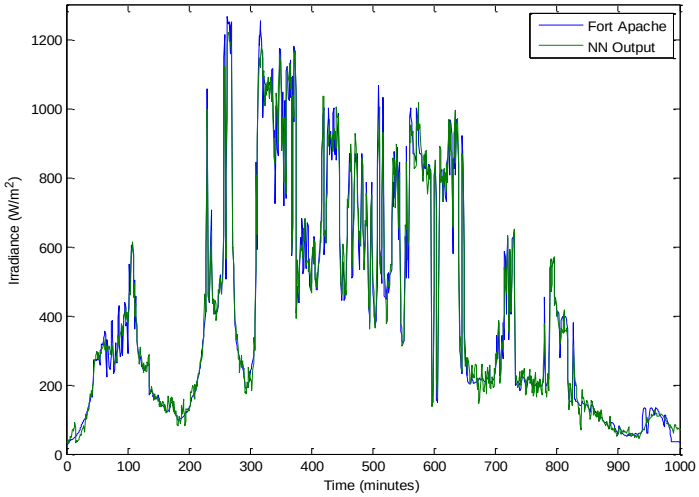


Figure 9. Measured and simulated (NN Output) irradiance for Fort Apache at 1 minute resolution for May 25, 2008.

After the model has been developed using known ground irradiance values, it can be implemented anywhere with satellite images. Current model results can be seen in Figure 10 for Fort Apache for the week after the training data. The model very accurately models the large transitions of the cumulous clouds later in the day, but has more trouble with the variability produced from the high thin cirrus clouds earlier in the day.

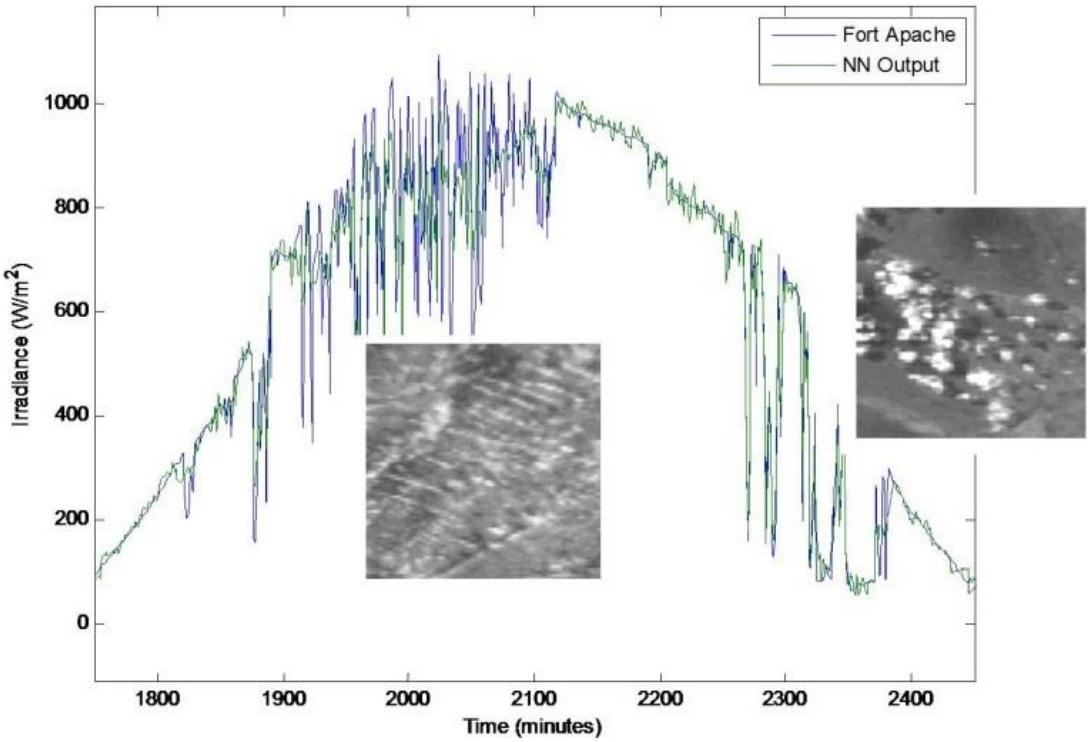


Figure 10. Measured and simulated (NN Output) irradiance for Fort Apache at 1 minute resolution for May 27, 2008.

A proof of concept model was developed in [55] to predict high frequency irradiance variability in areas with no ground sensors. Artificial Neural Networks (ANN) can be used to generate clear background images to do background subtraction, cloud identification, and cloud classification in satellite imagery. The ANN model has difficulty modeling all possible images to irradiance patters, but categorizing clouds and using separate neural networks for each cloud type could improve accuracy. The overall processing is very intensive and utilizing High Performance Computing Resources is necessary. For interconnection studies modeling solar power on the electric grid, a good model for system variability is needed. This method shows the possibility of modeling high-resolution solar variability using only satellite images.

2.3 Traditional Methods for Analyzing PV Interconnection Distribution System Impacts

The section provides a review of the traditional methods used to analyze the impacts of PV interconnections on the distribution system. First, the typical interconnection process that utilities go through for small scale PV systems is discussed. Second, a review is presented of the possible impacts that PV can have on the distribution system operation and control. Third, methods are discussed for analyzing how much PV can be interconnected on a feeder before there are issues, which is also called the PV hosting capacity.

2.3.1 Summary of Typical Interconnection Process

Distributed photovoltaic (PV) projects must go through an interconnection study process before connecting to the distribution grid. The interconnection study process is designed to identify possible system impacts and mitigation alternatives [2]. In the majority of the cases, system impacts can be ruled out or mitigation can be identified without an involved study, through a screening process or a simple supplemental review study [3]. For proposed projects that require a closer evaluation, expensive and time-consuming interconnection impact studies are required. A system impact study is performed to identify the potential electrical impacts associated with the integration of PV on the distribution system [4, 5]. Every PV impact study scenario is unique and often highly specific to the amount of PV generation capacity, feeder characteristics, and how much PV is already distributed along the same feeder. This can means each impact and mitigation strategy is location-specific. Another interconnection analysis challenge is the inherent variability in PV power output which interacts with feeder operation by affecting the operation of voltage regulation and protection devices.

For small systems (<50 kW), the PV interconnection application review and approval process is the single most time-consuming part of the process [59]. The median time for application review and approval is 18 days, and the mean is 27 days [59]. An approximate flow chart for the interconnection approval process is shown in Figure 11 [60, 61]. Many utilities use a standard small generator interconnection procedure (SGIP) process [62] for PV that includes an interconnection screen for placing requests into the simplified interconnection, or "fast track", that do not require more detailed study [3, 63, 64]. Most small residential PV system interconnection requests will go into the fast track. The traditional criteria for screening PV systems was 15% of the peak load of the feeder [63]. FERC has defined small generator interconnection procedures (SGIP) fast track eligibility using Table 1 [62]. Any system that does not meet the fast track eligibility will be required to have some supplemental review and possible detailed impact study.

Table 1. FERC Small Generator Interconnection Fast Track Eligibility [62].

Line Voltage	Fast Track Eligibility Regardless of Location	Fast Track Eligibility on a Mainline and ≤2.5 Electrical Circuit Miles from Substation
< 5 kV	≤ 500 kW	≤ 500 kW
≥ 5 kV and < 15 kV	≤ 2 MW	≤ 3 MW
≥ 15 kV and < 30 kV	≤ 3 MW	≤ 4 MW
≥ 30 kV and ≤ 69 kV	≤ 4 MW	≤ 5 MW

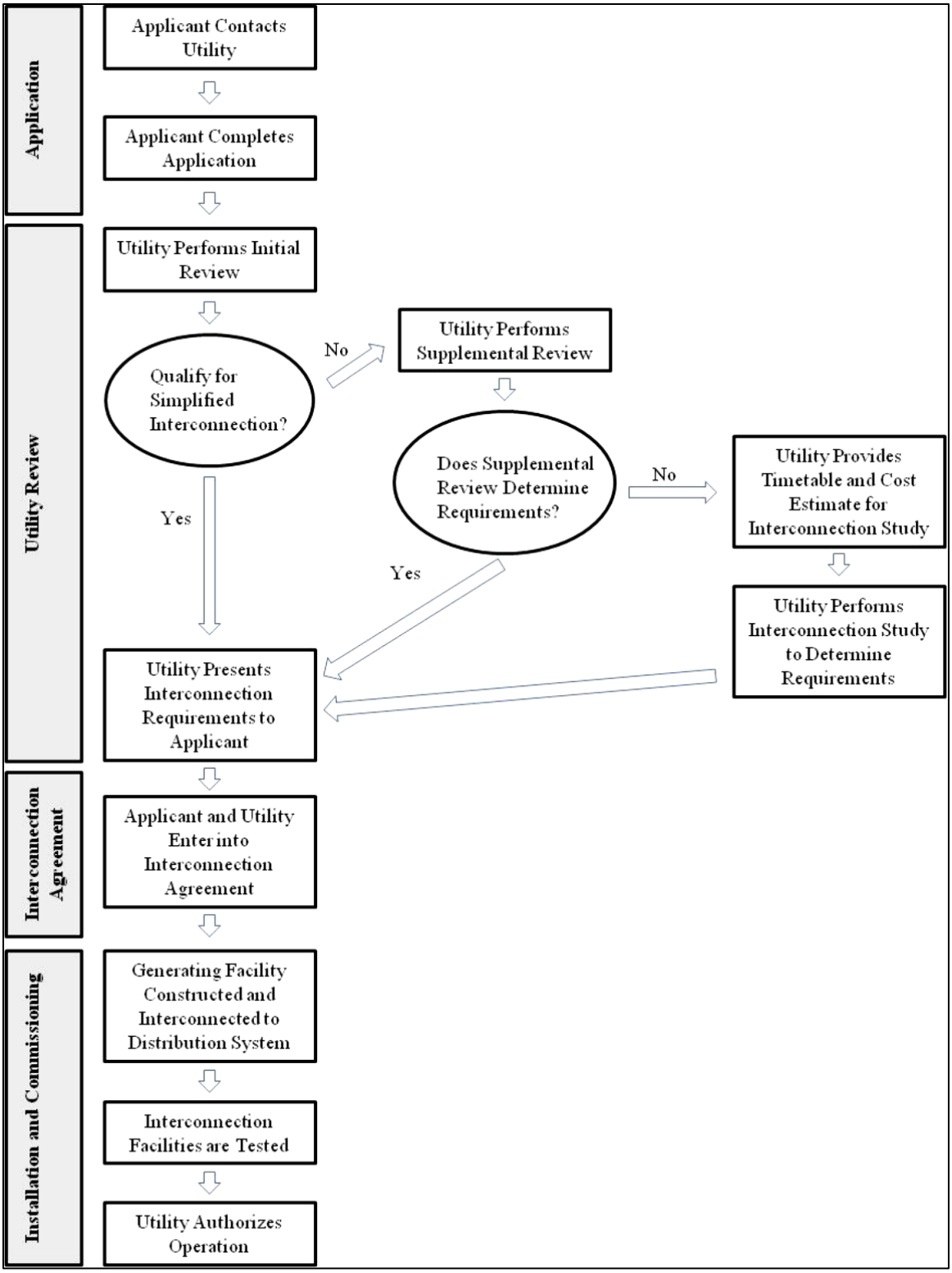


Figure 11. California Rule 21 Interconnection Process [60, 61]

2.3.2 PV Impacts on the Distribution System

Conventionally, distribution systems have been designed for voltage regulation and protection coordination considering one-way power flowing radially from the substation to the customers. As the adoption of distributed generation continues to rise, adding large amounts of distributed generation may cause two-way power flow, changing the historic paradigm and possibly impacting other customers on the distribution feeder [65]. Rooftop photovoltaic (PV) generation is one of the most common forms of distributed generation, and the variability and intermittency of solar power increases the challenge of grid operation. Two common concerns of PV interconnections are steady-state over-voltage [66] and line-loading violations [67]. PV can also cause issues with voltage regulation equipment [68], system losses [69], harmonics [70], voltage flicker [71], and protection [72]. PV interconnections must go through a screening process to investigate any such potential adverse effects of an interconnection [73].

One significant area of concern for interconnecting PV on the distribution system is the interaction with the voltage regulation equipment. Voltage regulators were designed for slow daily variability of the aggregate feeder load. The high variability and frequent changes in PV output over a long timescale can make the voltage regulation equipment continually change taps, creating additional degradation of the equipment [74-76]. Reactive power control of the PV inverters can be used to control the voltage locally [77], but without intelligent coordination, the PV reactive power injections can also create issues with the voltage regulation equipment [78, 79]. The impact to the number of voltage regulation equipment changes depends on the size of the PV system [80] and the position of the interconnection compared to the regulator [81].

2.3.3 Feeder PV Hosting Capacity Analysis

While PV interconnection impact studies typically investigate a specific location and PV size, another approach is to analyze the entire feeder and determine the feeder's PV hosting capacity. The results are feeder-specific, but they are generalizable to any PV interconnection location on the feeder. Using this approach, if the total installed PV on the feeder is less than the hosting capacity, regardless of location, there will be no significant impact to the grid operations. EPRI, along with a couple others [82, 83], has performed significant research in the area of feeder hosting capacity for PV [84-86]. Work has also been done to show how hosting capacity is a factor of the distribution parameters and can be increased with PV inverter reactive power control strategies [87-91]. The PV hosting capacity of a feeder can also be increased using demand management [92] and active distribution systems [93, 94]. Because hosting capacity and interconnection studies are generally specific to a given feeder topology, load level, or other feeder characteristics, the ability to interpret the results for a specific bus or feeder in a manner that generalizes this information for analysis is of interest.

2.4 Review of Circuit Reduction Methods

Many methods for circuit reduction have been published for different purposes, and some examples of circuit reduction techniques can be seen in [95-100]. These are often a reapplication of basic circuit analysis techniques to calculate circuit parameters for a simpler representation. One key circuit equivalencing technique that deserves special attention comes from the Western Electricity Coordinating Council (WECC) guideline for modeling wind power plants [101]. WECC published a similar guideline for modeling PV systems in large-scale load flow simulations based on the wind guideline [102]. Both WECC guidelines use the same method of approximating the

equivalent impedance for a single-machine representation, and it is also well established in other literature [103, 104].

The WECC equivalencing method was first published for reducing a collector system of a large wind power plant [105]. The method reduces a multi-machine system with varying impedances between the collector and the wind turbine generators to a single equivalent machine and single equivalent impedance representation. The single machine represents the average conditions on the wind power plant, and the single equivalent impedance is the average impedance weighed by the square of the current. This method was formulated to produce real and reactive line losses equivalent to the full wind power plant network. The equivalent impedance of the wind power plant is the sum of the individual line losses (current^2*impedance) divided by the square of the total current being produced by the wind power plant, I_{total}. For each line with impedance Z_m and current I_{Zm}, the equivalent impedance for a collector with n line segments is

$$Z_{eq} = \frac{\sum_{m=1}^{n} {I_{Zm}}^2 Z_m}{{I_{total}}^2} \quad (1)$$

.

The simplest implementation of this method assumes that all turbines have the same power output and rating, so the I_{Zm} terms in (1) for current can be represented by the number of downstream turbines and I_{total} is the total number of turbines [105]. The more advanced method uses the actual current in the lines to allow for different turbine or inverter ratings [106]. The WECC literature proposes a method similar to a DC power flow to calculate the line currents I_{Zm} in (1). DC power flow is commonly used in a simplified model of the power system network as a rough approximation for such tasks as production costing and trading optimization because of the speed and simplicity of the calculation due to disregarding reactive power, voltage levels, and active power losses. Since all voltages are fixed, it is a system of linear constant equations that can be solved without iteration. The WECC method can use this approximation, along with the fact

that it is a radial network, to approximate I_{Zm} by hand without solving the full power flow or having to form the Y_{bus} impedance matrix. It is important to remember that this method of calculating line currents is an approximation because the line losses make the assumption of equal bus voltages false, but it is not a bad approximation since the variation in voltages is small. If the simplified DC power flow is used, the equivalent impedance is slightly different than the exact equivalent impedance. When compared to the full plant representation, this simplified model varies slightly with regard to plant short-circuit contribution as well as the power angle with reference to the grid. The method provides an easy-to-calculate approximation that can be done by hand, and has been shown to work well for wind transient and stability studies [107] and for evaluating wind farm harmonics [108]. Errors for reactive power loss can be higher than active power errors because of the assumption that reactive power generated by the line capacitive shunts is at one per unit voltage [105]. In [109] it is shown that the WECC single turbine representation does not perform well under some conditions of diversity in line impedance, diversity in power production, or diversity of generation types. The WECC method allows both active and reactive losses to be approximated by hand. The approximation in the WECC method is in the calculation of I_{Zm}, so if higher accuracy is required, the full wind or solar plant information along with the entire collector information can be entered into a power simulation package to solve for the full power flow.

The WECC equivalencing method is designed for studying the impact of large plants on the bulk electric transmission system, and it cannot easily be used to tackle the system in Figure 12 because of the diversity of loads and generators. The objectives of the WECC method did not include interest in the voltages or details inside the feeder, only their impacts on the transmission system. Once the circuit is reduced to an equivalent "average" load and "average" DG shown in Figure 12, the model does not provide any information about the voltage deviations or extreme voltages inside the

distribution system that are valuable for studying the impact of DG on the distribution system. The WECC model was never intended to be applicable to this case. To study the impact of PV on the distribution system, the equivalent circuit must preserve the locational value of solar with impacts to specific parts of the feeder and correctly model voltages inside the feeder, especially at locations with voltage regulation equipment.

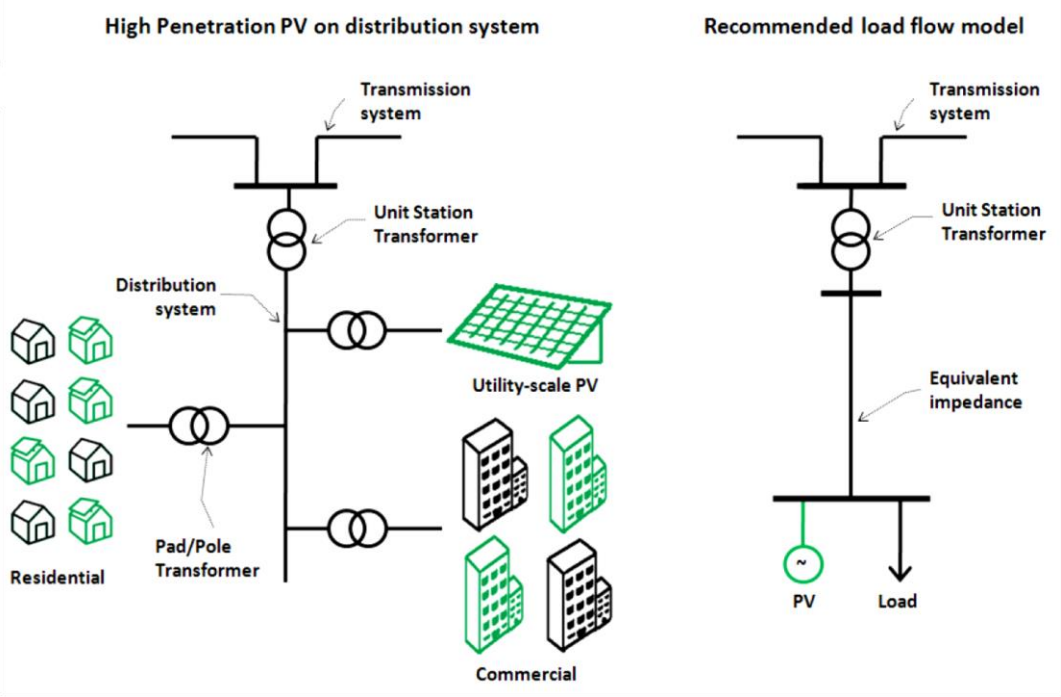


Figure 12. WECC model for distributed PV [102].

The WECC model is useful for quickly approximating the equivalent impedance for a single-machine representation of a large wind power plant or a large PV plant. This could be used for modeling large central PV systems interconnected on the distribution system, but reducing the entire feeder would lose details necessary for distribution system interconnection impact studies. Because the method assumes fixed voltage on all buses, it probably would not work well for equivalencing large distributed PV systems connected on the secondary system of the distribution system where the voltage varies significantly at locations around the feeder. The WECC equivalent impedance also requires all line currents to change in proportion to one another through time. This is a

good approximation for a large wind power plant or large PV plant where all inverters in the plant increase or decrease together in time, but it is more complicated to apply to distributed rooftop solar, especially with dispersed loads in the feeder each with different load shapes through time.

Another method called the exact lumped load model was specifically developed to reduce the complexity of loads on the distribution system [110]. The reduced circuit model includes the extreme feeder voltages by modeling the voltage drops in the circuit. This method assumes that all loads are constant current loads and are uniformly distributed along a line in the feeder with equal spacing and equal magnitude. The uniformly distributed requirement is a big assumption and limitation of the method, but this is most commonly the case on single phase laterals where equally rated transformers are regularly spaced along the lateral. The method could also be used for large PV plants where equally rated inverters are equally spaced throughout the plant. The exact lumped load model ensures that the voltage drop to the end of the line is the same in the reduced model and that the line losses are equal. For simplification and approximation, the model is developed for the case where the number of loads goes to infinity and the distance between the loads goes to zero. With these assumptions, the resulting model for a feeder with length l and total feeder load I_T is shown in Figure 13.

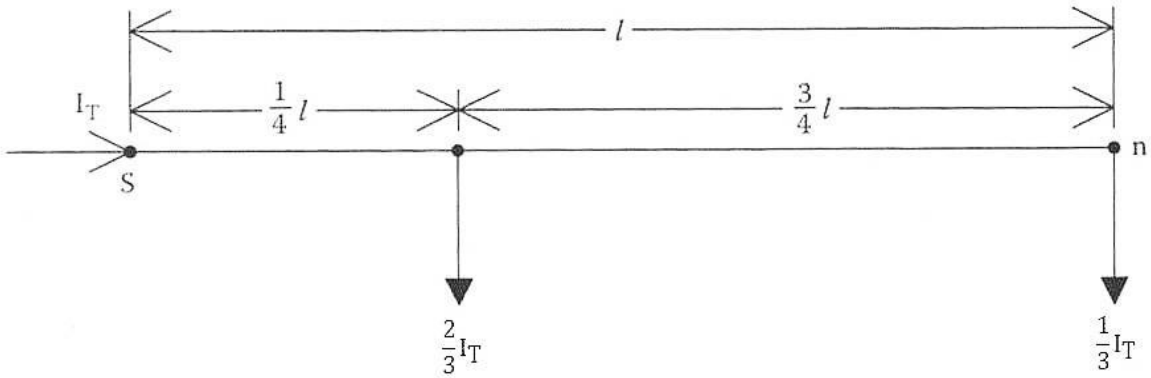


Figure 13. Kersting exact lumped load model [110].

The exact lumped load model is useful in specific circumstances with uniformly distributed loads, or it can provide a reasonable assumption for line losses and voltage drop along a feeder if the load sizes or locations are unknown. In contrast, if a simplified equivalent circuit for a full distribution system model is required, the exact lumped load model does not capture the diversity of line impedances and load sizes. Specific sections of the feeder may be applicable to use the exact lumped load model, but the model could not provide an equivalent representation for an entire feeder due to the complexity of load sizes (residential, industrial, commercial), range of line lengths in the feeder, and variety of possible distributed rooftop PV sizes.

Several existing circuit reduction methods have been discussed, along with their weaknesses. In Chapter 4, a new algorithm is proposed for simplifying distribution system models for faster PV interconnection analysis.

CHAPTER 3: TIME-SERIES APPROACH FOR DISTRIBUTED PV SIMULATIONS

3.1 Introduction

To examine the impact of PV on the distribution system, many different types of studies and analyses can be performed. Commercial circuit analysis tools have historically provided the capability to perform steady state power flows to analyze the distribution system at specific snapshots in time, but PV output is highly variable and the potential interaction with control systems may not be adequately analyzed with traditional snapshot tools and methods. Highly detailed and accurate interconnection impact studies require a time-series simulation with large amounts of high-resolution data.

This chapter discusses several aspects of quasi-static time series (QSTS) simulations and how high time-resolution data can be used to assess the potential impacts of PV on the distribution system in a more comprehensive manner. The main advantage of using QSTS simulation is its capability to properly analyze and capture the time-dependent aspects of power flow [111-114]. QSTS produces sequential steady state power flow solutions where the converged state of each iteration is used as the beginning state of the next. Examples of the time-dependent aspects of power flow include the interaction between the daily changes in load and PV output and the impact on voltage regulation equipment. QSTS analysis is also commonly used to study the impact of plug-in electric vehicles on the distribution system [115, 116].

All electrical modeling is done in the open source software OpenDSS from EPRI [117]. OpenDSS is commonly used to model solar on the grid because of its timeseries capabilities [118-120]. The program was designed to help distribution planners analyze

various issues with distributed generation. All power flows were solved with OpenDSS and the results transferred to MATLAB through a COM interface [121].

3.2 Simulation Data Requirements

The application of QSTS simulations requires more data to represent the time-varying PV output coincident with time-varying load. The necessary data set can become very large depending on the resolution and length of simulation desired. Any time that large datasets are used, there will be significant effort required for cleaning, processing, and validating the accuracy of the data. QSTS simulation introduces new and more complex data requirements for power flow simulation. The data requirements for QSTS can be divided into three categories: model data, load data, and PV data.

The implementation of QSTS may require the gathering of additional distribution system model data, including time delay control settings on voltage regulation devices such as capacitors and VREGs. The details of voltage regulation controls, such as reset modes and delays, are not necessary for snapshot power flow simulations, but this information becomes critical for accurate timeseries analysis results.

QSTS simulations require the availability of historical time series load data that is often not easily available at the required time resolution for the scenarios or study of interest. It is common for utilities to record feeder level load data at 15-minute or 1-hour resolution, but these time resolutions may be too low to analyze some aspects of PV system impacts that function on the order of seconds. For example, to study voltage regulator tap change operations, it is typically necessary to perform simulations at a 1-second resolution, which requires 1-second PV and load data. The most straightforward approach is to linearly interpolate the load data to a higher resolution. This will capture the long-term, e.g. 15-minute, variability effects of load, but it neglects any short-term variability. In [122], the authors propose a method to synthesize high resolution (1-

second) load using an autoregressive function from some historical load data measurements.

The most ideal input for PV QSTS simulations is high resolution irradiance data locally measured at the feeder time-coincident to the load data measurements, but there are very few 1-second resolution irradiance data sources in the United States. Commonly, either low resolution data is used for the analysis, or high resolution data from a distance geographical location is transformed to the study location. Using a basic diurnal PV output pattern, such as a clear sky model [13], could still provide some valuable insights to potential interactions between the load and PV generation. When using high resolution irradiance data, it is important to correctly model the reduction in variability of the PV power due to the geographical smoothing that will occur over the area of the PV plant. Methods like the Wavelet-based Variability Model (WVM) can be used to estimate the PV power output using an irradiance point sensor [7, 123, 124].

3.3 Time Series Power Flow Analysis

Two time series power flow analyses are demonstrated in this section to provide an example of QSTS interconnection analysis. A more detailed discussion on performing PV interconnection studies and additional analysis examples is shown in [73]. The feeder in Figure 14 has a substation LTC with LDC and two switched capacitors. The substation transformer serves a total of four feeders, and the other three feeders were simulated as lumped loads.

The first analysis investigates operations of voltage regulation equipment during a 9-month simulation with the central PV system connected at the furthest three-phase point on the feeder that could thermally support the PV plant. Coincident feeder load data and local high resolution irradiance measurements are used for the simulation. The hypothetical PV plant has a nominal capacity of 7.5 MVA output at unity PF, which is equal to 100% of feeder peak load. The simulation was run at 1-second resolution from

January 1, 2011 through September 30, 2011. Table 2 shows a comparison of the base case and PV case with regard to LTC and switched capacitor operations for the 9-month simulation.

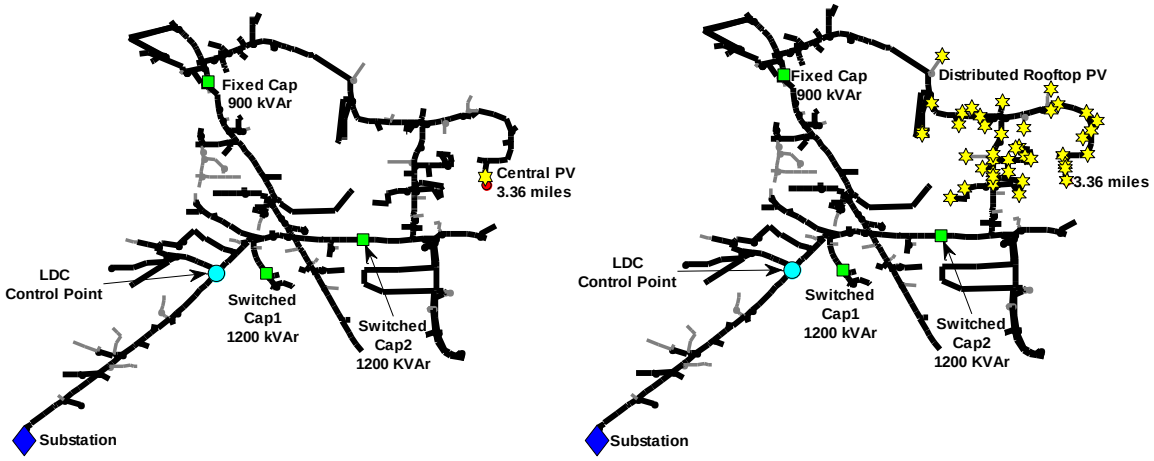


Figure 14. Distribution feeder with one central plant or distributed rooftop PV

Table 2. Device Operation Comparisons for the Base Case and PV Case.

Device	Operations Base Case	Operations With PV (Differential)	Percent Change
LTC	459	394 (-65)	-14%
Cap 1	12	6 (-6)	-50%
Cap 2	16	28 (+12)	+75%

The addition of PV resulted in a net reduction in operations observed over the 9 months for the LTC and Cap 1 (nearest the substation) and an increase in the operations for Cap 2. The substation LTC is a ±8 step device, unlike the more common ±16 step devices, which means that each tap change results in twice the voltage change per step and fewer operations. Figure 15 shows a column plot with the total LTC operations by month for the 9-month simulation of both the base case and PV case. The differences shown in Figure 15 highlight the periods where PV causes the greatest decrease in operations, which is during the summer months, and a small amount of additional operations, which occurs in the winter months.

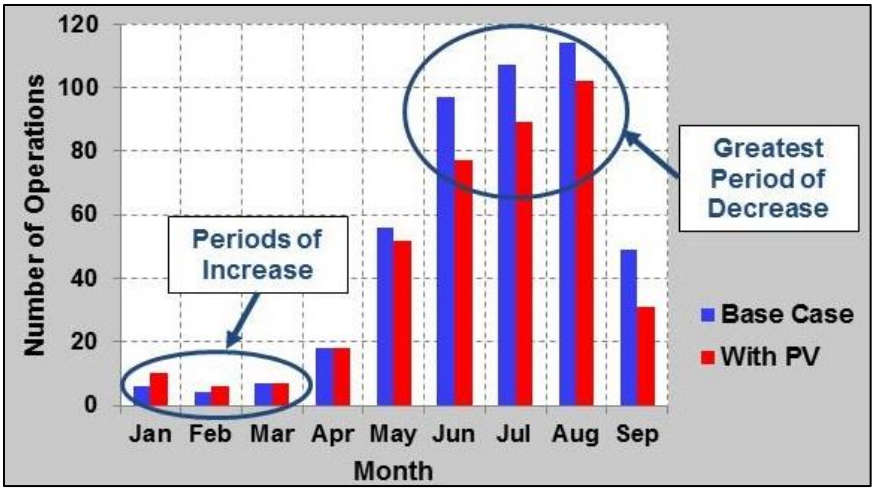


Figure 15. LTC Operations by Month, Base Case and With PV, 9-Month Simulation

Note that the distribution system is connected to a stiff 115 kV transmission system. This means the number of LTC operations will be lower than an LTC connected to either a weaker grid (low short-circuit current) or a lower voltage transmission system. The LTC is connected to three additional distribution feeders, so a high penetration of PV on one feeder may not considerably affect the substation current or the number of LTC operations. PV variability can have a more significant impact on distribution system LTC's for a weaker grid and when there are fewer feeders on the transformer.

The second example uses the distributed rooftop PV shown in Figure 14 to analyze the PV's impact to the distribution system voltages. The simulation was run for a week surrounding Saturday, April 23, 2011, at 1-second resolution. The total nominal output of the distributed rooftop PV is 7.5 MW, and each PV system is connected on the secondary system. Figure 16 shows the total aggregate power output of the distributed rooftop PV systems at the end of the feeder in comparison to the substation and feeder real power. A check for voltage issues was performed as part of the analysis to verify the highest and lowest voltage found at any location on the feeder during the week. This allows for a thorough check to determine if further study is necessary and to identify the location of the highest and lowest voltages, both with and without PV. Figure 17 shows the plot of the highest and lowest voltages for the PV case during the study week.

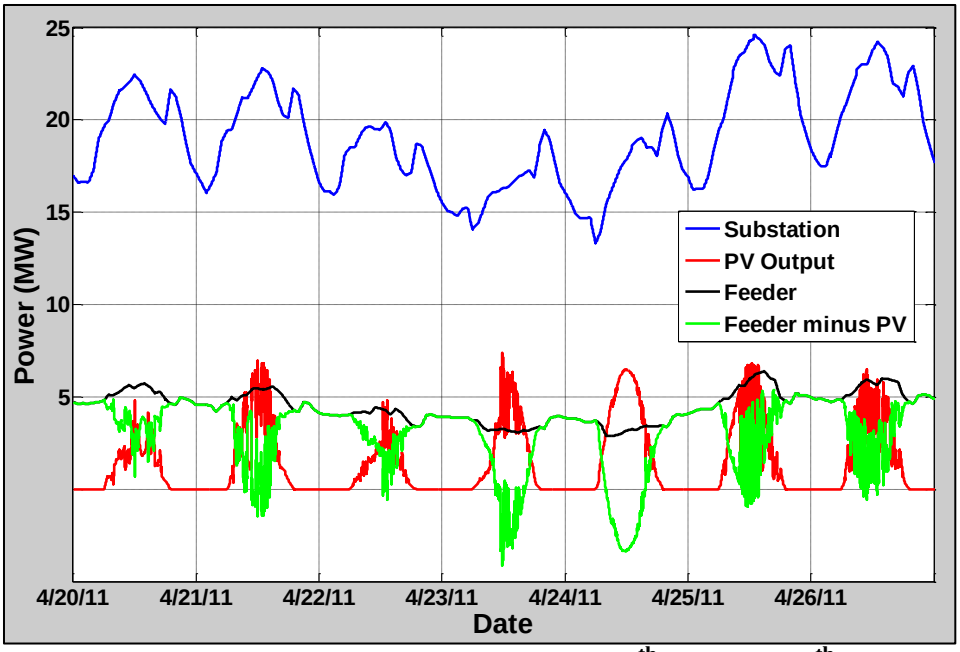


Figure 16. Power profiles for April 20th through 26th

Figure 18 shows the feeder voltage profile at the time of highest voltage identified. Figure 18 shows all phases and lines on the feeder, with secondary services shown as dashed lines. This illustrates the extreme voltage rise observed on the secondary with PV and the location of the highest voltage. This example illustrates the importance of considering secondary voltage rise to PV systems.

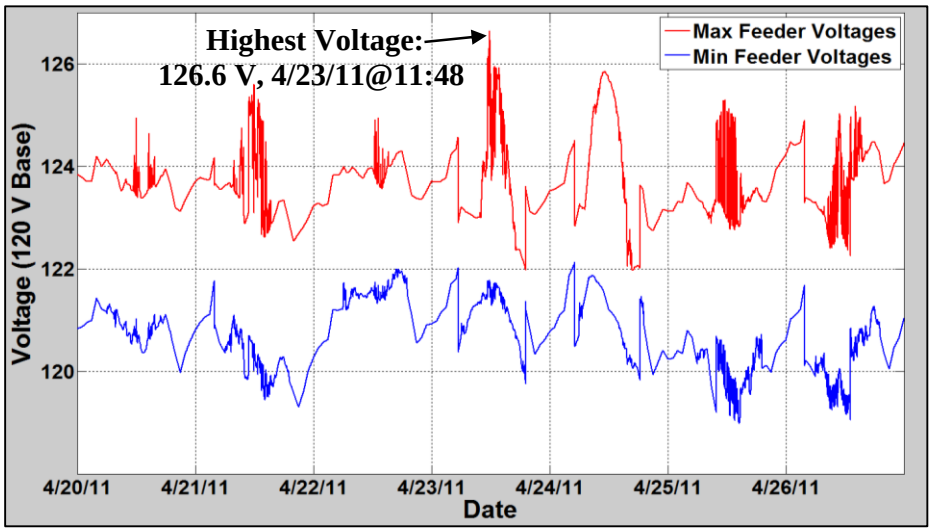


Figure 17. Maximum and Minimum Voltages with PV for Study Week

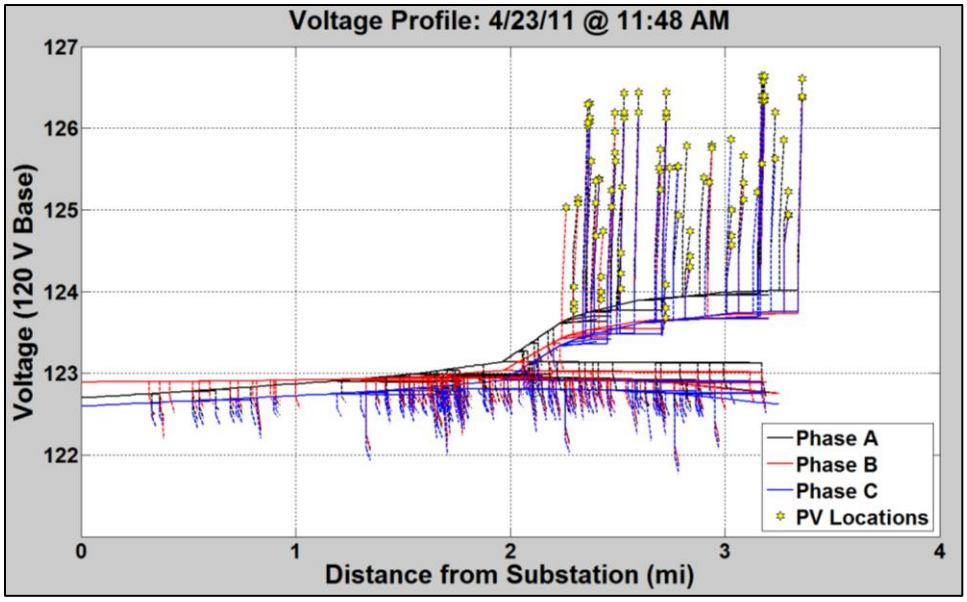


Figure 18. Voltage profile for the feeder during the highest voltage time

Distributed PV interconnection studies using time-series simulation and high time-resolution data can better characterize the specific impacts of high deployment levels of PV systems on the distribution system. Because PV output is highly variable, the potential interaction with control systems is not adequately analyzed with traditional snapshot tools and methods, which only provide an assessment of the distribution system at one instant in time. Some brief examples were shown here and the full details and methodology can be found in [73].

3.4 Impact of Time Step Length and Interpolation Methods

The load data for the feeder shown in Figure 14 is at 1-hour time resolution. In order to run a simulation at a finer resolution than 1-hour, the load data must be converted to a higher resolution. The simplest method for this is to interpolate from the 1-hour data to any desired resolution. While this does not fully represent the variability in the load, adding variability synthetically and accurately modeling the load without more detailed data can be difficult. This section is dedicated to investigating the impact to the simulation results by using different interpolation methods for the load data. The

impact of running the simulation at differing time resolutions and power flow control modes are studied.

The impact of different interpolation methods was studied by comparing the number of load tap changer (LTC) operations using each linear interpolation, cubic spline interpolation, nearest neighbor interpolation, and piecewise cubic Hermite interpolation of the load data. The results are shown in Table 3 for a 1-month simulation of the 30 day period with the most LTC operations (08/02/11-08/31/11). Note that each interpolation method produced very similar results, but there are slight differences all within ±2 operations for different interpolation methods. This provides a feel for the range of error and certainty of the tests, with differences of 1 or 2 operations between simulations being statistically insignificant because they are within the error bar from differing valid assumptions of interpolation. Although the capacitors act once more during the month period for nearest neighbor interpolation, the results are not anomalous and no conclusions should be drawn.

Table 3. Comparison of the number of switching operations during a 1-month simulation in time control mode with different simulation time resolutions and load interpolation methods.

Resolution	Linear Interp			Spline Interp			Nearest Interp			Cubic Interp		
	LTC	Cap1	Cap2	LTC	Cap1	Cap2	LTC	Cap1	Cap2	LTC	Cap1	Cap2
1 second	101	0	0	101	0	0	101	2	2	101	0	0
30 second	101	0	0	101	0	0	101	2	2	101	0	0
1 minute	101	0	0	101	0	0	101	2	2	101	0	0
5 minute	101	0	0	101	0	0	101	2	2	101	0	0
15 minute	99	0	0	101	0	0	101	2	2	101	0	0
30 minute	97	0	0	99	0	0	97	2	2	97	0	0
1 hour	83	4	2	83	4	2	85	4	2	83	4	2

A decrease in LTC operations for the 30-day simulation can be observed in Table 3 as the time resolution increases to longer periods. This is explained by the method OpenDSS uses to control the voltage regulators in the “time” control mode. In the

simulated distribution system, each of the control devices (LTC, Capacitor 1, and Capacitor 2) has a time delay of 30 seconds. OpenDSS detects when the voltage goes out of band and a control operation should occur. In "time" control mode, OpenDSS starts a counter of 30 seconds, and a tap change occurs if the voltage is still out of band at the end of the delay. The issue with long simulation timesteps like 30 minutes is that OpenDSS does not check the voltage when the 30 second counter expires. Instead, it only evaluates the state of the system and control actions when the power flow is solved, which could be 30 minutes later. If the simulation time resolution is long, the state of the system is less likely to still be out of band when the system is next solved, so the number of operations decreases as the time step lengths are increased. Longer time resolutions have a similar affect as lengthening the time delays on the control actions. The 1-hour time resolution also produces several more capacitor operations that were not observed on higher time resolution simulations. This appears to be in the control logic of OpenDSS. At a 1-hour timestep, both the capacitors and LTC can be out of band at the end of the timestep. In this simulation, when OpenDSS solves the state of the system, if both the LTC and capacitor are out of band, OpenDSS activates the capacitors first after the 1-hour period, and then changes the LTC tap if it is still out of band after activating the capacitor and resolving the state of the system. In "time" control mode, we recommend using a simulation time resolution with no greater time than the shortest time variable in the system. For example, if the time delays are 2 minutes, then a 2-minute time resolution could be used.

To resolve the issue of OpenDSS not checking the control action counters until the next solved timestep, OpenDSS also has a "static" control mode for solving the power flow. In this case, it is essentially the same as setting the time delay on all control actions to zero. For high variability conditions, this would create a very large number of control actions anytime there was a momentary out of band voltage. For this reason, running the simulation in "static" mode during the daytime with variable solar power would not be a

valid option. Without PV or at nighttime, the state of the system is solely determined by the system loading. As previously discussed, the load is at a lower resolution (15 minute to 1 hour resolution). With linear interpolation, all extreme points of the load and the system will occur on the load datapoints, which means a lower time resolution can be used. The "time" control mode has the issue of delayed control actions, but "static" mode correctly solves the 30-day simulation even at a 1-hour resolution as shown in Table 4.

Table 4. Comparison of the number of switching operations during a 1-month simulation with linear load interpolation with different simulation time resolutions.

Resolution	Time Control			Static Control		
	LTC	Cap1	Cap2	LTC	Cap1	Cap2
1 second	101	0	0	101	0	0
30 second	101	0	0	101	0	0
1 minute	101	0	0	101	0	0
5 minute	101	0	0	101	0	0
15 minute	99	0	0	101	0	0
30 minute	97	0	0	101	0	0
1 hour	83	4	2	101	0	0

3.5 Impact of Smart Inverters in Time-series

As the penetration level of PV on the distribution system grows, the current injection by PV can create over-voltage issues around the location of the interconnection of PV. Often, the voltage regulation in the feeder is not setup to handle these reverse current flows and inverse feeder voltage profile shape. Smart inverters have the potential to change their reactive power generation or consumption based on time of day, interconnection voltage, or real power generation. These smart inverter functions are implemented and simulated in time-series to understand the inverter's capability to impact feeder voltage with variable PV output.

With deployment of distributed PV systems increasing rapidly, interconnection studies have shown that high voltage conditions can occur on the distribution system, especially under conditions of high penetrations of PV and when a large PV plant is connected to the end of a feeder [1, 5, 73]. An example of high voltages due to PV is shown for the distribution feeder in Figure 19 with a 7.5 MW central PV plant (100% of feeder peak load). The feeder has a load tap changer (LTC) at the substation with load drop compensation (LDC) and has two switched capacitors. The central PV system is connected at the end of the feeder on the furthest three-phase point that could thermally support a 7.5 MW PV plant. The simulation was run for the peak penetration week of April 20, 2011 to April 26, 2011 with coincident load and local irradiance data. The simulation uses substation load data measured hourly and irradiance data measured at 1-second resolution in the middle of the distribution feeder. The irradiance data was transformed to power output of a 7.5 MW central PV plant by using the wavelet variability model (WVM) [123]. This feeder and time simulation will be used throughout this section to demonstrate options for mitigating the high voltages using smart inverter functionality.

Figure 20a shows the maximum and minimum voltage anywhere on the feeder for each second of 4/23/2011, demonstrating the range of voltages. The red line in Figure 20a is the maximum feeder voltage plotted through time with the 7.5 MW PV plant at unity power factor. The maximum voltage occurs at 11:48:19 on 4/23/2011, or hour 83.8 on the simulation hour timescale. The voltage profile plot along the entire feeder with the 7.5 MW PV plant is shown in Figure 20b. Note that the voltage increases along the feeder to the PV plant at the end. In Figure 20b, the dashed lines represent the voltage drop in the secondary transformers and secondary system. This simulation shows how high penetrations of PV at unity power factor can create issues by increasing voltages around the PV.

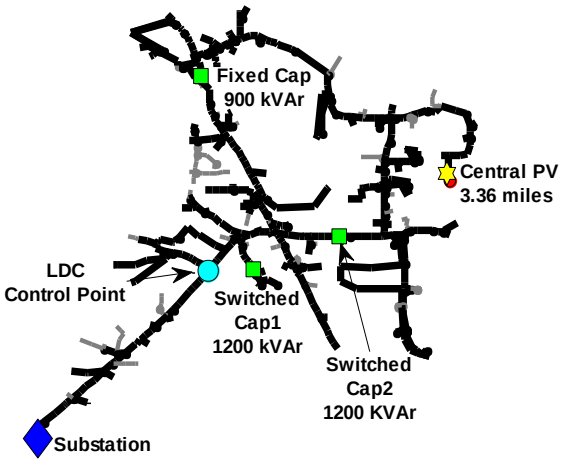


Figure 19. Feeder circuit map used for simulating 7.5 MW central solar plant.

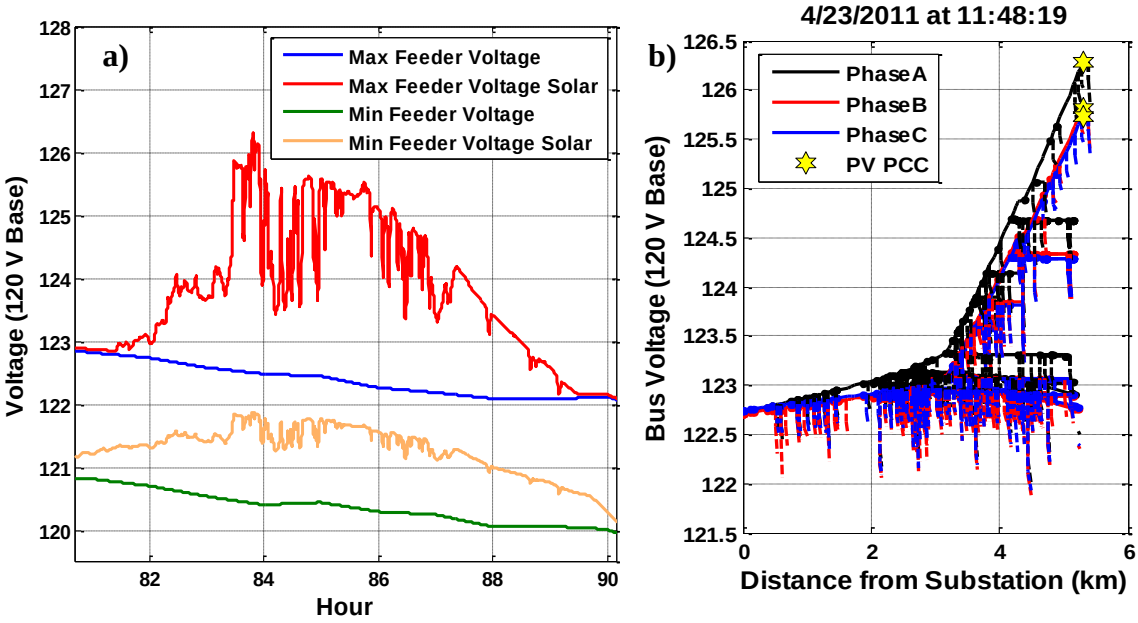


Figure 20. A 7.5 MW central solar plant at unity power factor for a) the fourth day (4/23/2011) of the simulation with b) the over voltage condition occurring at 11:48:19

Voltage regulation equipment can be used to control the voltage, but solar variability can create frequent tap changes, which puts increased wear on the equipment [68]. A common solution to the high voltage issues from PV systems is to adjust the power factor to absorb reactive power. Due to the line impedance between generators and loads, voltage is commonly regulated using reactive power output control. Smart

inverters can also be operated where reactive power is generated or absorbed to increase or decrease the voltage. The main purpose of the solar inverter is still to generate real power (kW) from the solar irradiance on the PV panels with the normal control logic, but additionally any remaining capacity of the solar inverter can be used to output reactive power (kVar) to regulate the voltage.

As shown in Figure 21, even a slight change in the PV output power factor to 0.95 decreases the voltage at 11:48:19 from 126.3V to 123.4V at the PV point of common coupling (PCC). Literature includes extensive discussions about the impact to the distribution system caused by absorbing volt-ampere reactive (Var) and changing the power factor on distributed resources with different possible power factor control strategies [120, 125, 126].

The var output of the inverter can be controlled many different ways. A fixed, constant-var output could be specified to always output the same reactive power. Alternatively, a schedule could be specified to vary the var output by time of day. Furthermore, because the kW output of the solar inverter increases the voltage at the PCC, the kVAR output could also be specified as a function of the kW output. Finally, the var output of the inverter could be controlled based on the voltage at the PCC.

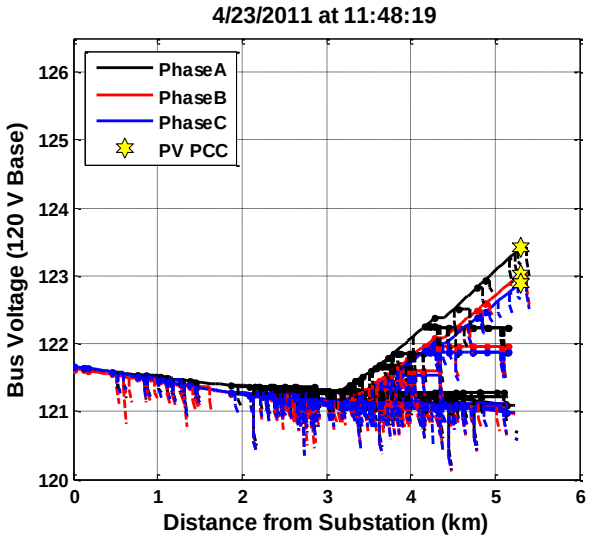


Figure 21. Simulation with 7.5 MW central solar plant at 0.95 leading power factor for 4/23/2011 at 11:48:19.

Figure 21 shows a specific case where a PV system with a leading power factor decreased the voltage. To analyze the general impact of power factor on voltage, Figure 22 shows the PV PCC voltage for the fixed instant in time (4/23/2011 at 11:48:19) with the 7.5 MW PV output at varying power factors. This demonstrates the exact impact that the power factor of the PV output has on the distribution system voltage. With a leading (absorbing) power factor, the voltage at the end of the feeder decreases, and with a lagging (producing) power factor, the voltage increases.

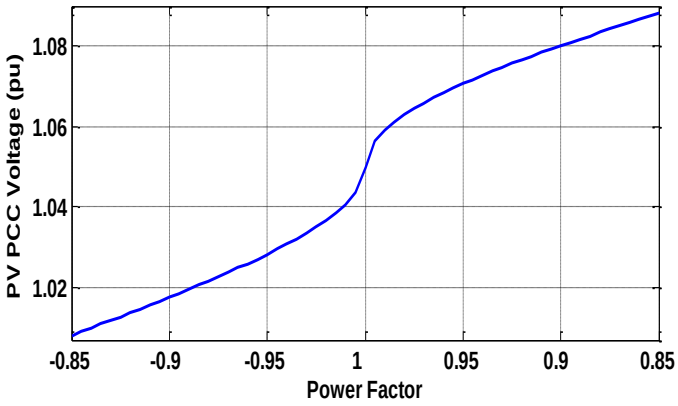


Figure 22. Voltage (pu) at the PV PCC on 4/23/2011 at 11:48:19 for different PV output power factors for the 7.5 MW PV plant

Generally, as the PV output power increases, the voltage rises at the PV PCC because of impedance between the PV system and the closest voltage regulation equipment. As shown in Figure 22, the PV PCC voltage is also a function of PV output power factor. An analysis of the PV PCC voltage as a function of both output power and power factor for 4/23/2011 at 11:48:19 is shown in Figure 23.

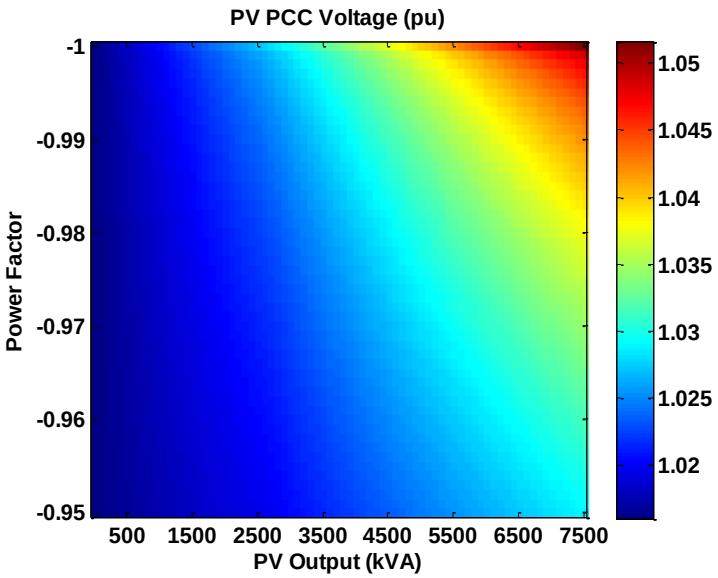


Figure 23. Voltage (pu) at the PV PCC as a function of PV output power and power factor for 4/23/2011 at 11:48:19

Other than the fixed lagging power factor previously mentioned, two other possible control strategies are proposed for adjusting the output power factor without voltage measurements. The first power factor control strategy is to adjust the power factor by time of day. If the distribution engineers know from experience that high voltages occur on the feeder at specific times of day, either from the solar output or the load, the power factor of the PV can be decreased during these times. An example is shown in Figure 24. This example simply decreases the power factor when the solar production is expected to be the highest in the middle of the day. The solar inverter could also be set to output Vars at certain times of day to support the voltage.

The power factor schedule shown in Figure 24 was used to run the same peak penetration week simulation with the 7.5 MW PV plant at the end of the feeder. The simulation results are shown in Figure 26 for this power factor schedule. This power factor schedule is advantageous because in the mornings and evenings when the solar output is low the solar output is at unity power factor, which helps support the voltage.

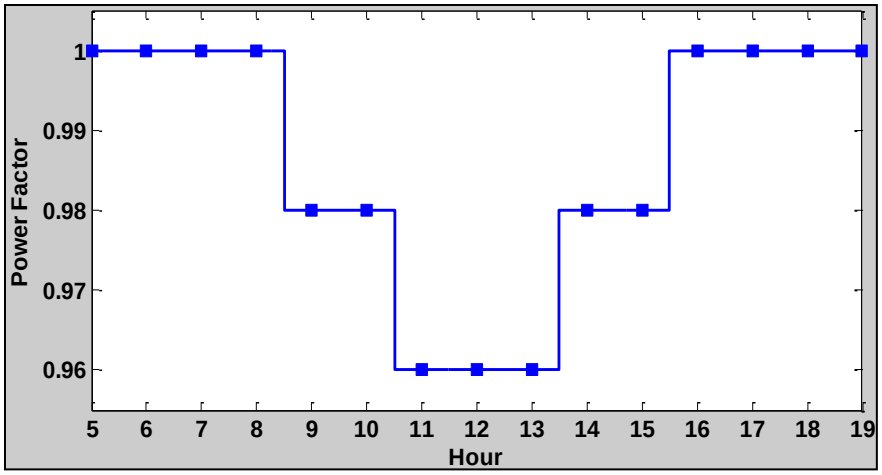


Figure 24. Example power factor schedule

The second power factor control strategy shown is controlling the power factor as a function of PV output power. In Figure 23, the PV PCC voltage is shown to be a function of PV output, so the PF can be designed as a function of PV output to counteract the voltage increase. Because a detailed simulation cannot be completed for every PV plant being installed, a generic function for power factor like that shown in Figure 25 can be used. Similar to the concept for the power factor schedule, the power output is at unity power factor for lower solar outputs, which helps support the voltage and produces the most energy. Some authors such as [127] have proposed also making this a function of the *X/R* ratio at the point of interconnection.

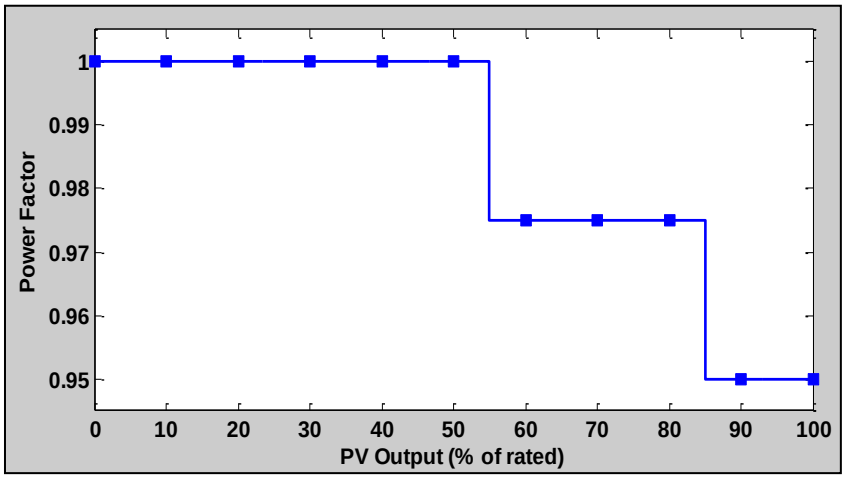


Figure 25. Example of power factor as a function of PV output

The simulation was run with the 7.5 MW PV plant at the end of the feeder and the power factor function from Figure 25. The results in Figure 26 show lower voltages than when the PV plant is at unity power factor. The advantage of the power factor function is that it is directly proportion to the solar output, instead of assuming a certain amount of solar power at each time of day. The three methods (fixed power factor, power factor schedule, and power factor function) are graphed together in Figure 26. These example control methods all bring the maximum feeder voltage within the appropriate limits.

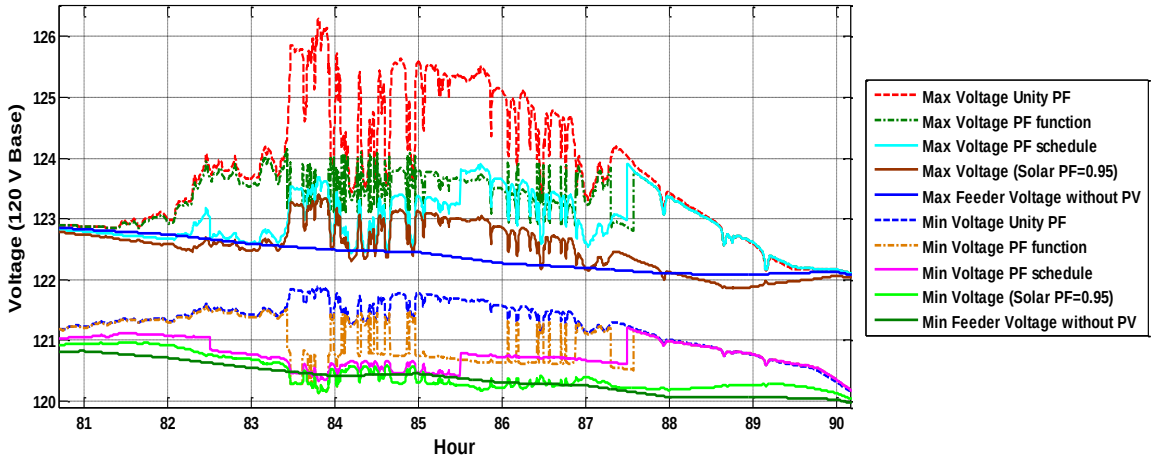


Figure 26. Feeder voltages with varying ways of modifying solar output power factor (PF)

Other authors have studied the implementation and impact of Volt/Var control [120, 128] and investigated distributed optimal control strategies for reactive power [129-131]. As indicated in Figure 27, to assist in regulating voltage, the reactive power generation from the PV inverter is varied from capacitive to inductive depending on the PCC voltage. When the voltage is around the nominal or desired voltage, the solar inverter does not output any reactive power. The amount of reactive power that the PV inverter can generate depends on the real power generation. In Figure 27, the y-axis must be dependent on the "headroom" in the inverter kVA rating left after subtracting the active power being produced. Using a curve like this, even at a single system voltage on

the x-axis, the reactive power generated may vary due to solar irradiance variability and changes to the inverter headroom.

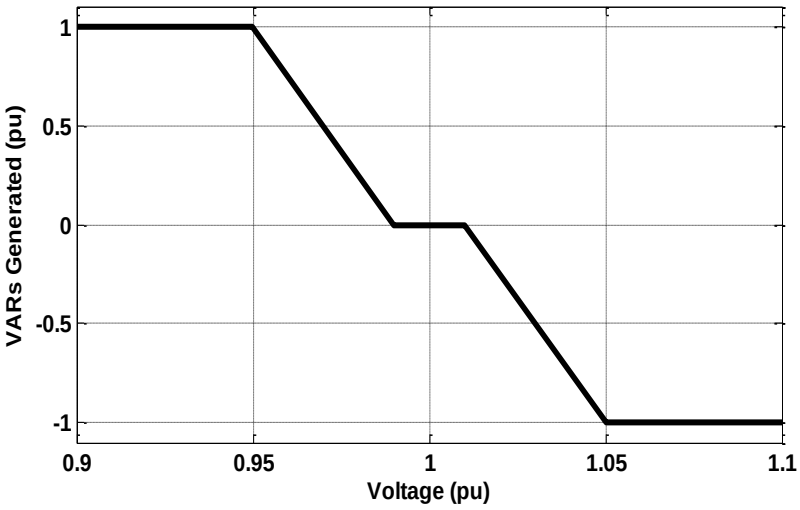


Figure 27. PV volt/var control curve with deadband.

The OpenDSS simulation software includes a control module for changing reactive power generation based on voltage described in [120]. In OpenDSS control elements are modeled separately from the standard power delivery or conversion elements. The solution algorithm is an iterative process of solving the power flow and allowing the control elements to take action. Thus, volt/var control decisions and actions are executed only on converged power flow solutions rather than during the power flow iterative process. The iterative process also has the advantage that the final solution for each time-step involves taking control actions immediately, instead of applying them after the power flow solution for the next time-step.

As an example of the volt/var control features, the control was simulated for the distribution feeder in Figure 19. The peak penetration week was simulated with results being shown for 4/20/11. A day was selected with variable irradiance to fully demonstrate volt/var control. The simulated real power plant output is the same in each simulation and can be seen in Figure 29. The PV connected at the end of the feeder is simulated for three different scenarios: unity power factor solar output, volt/var control

shown in Figure 27 with a deadband around the voltage, and PV inverter performing full voltage regulation.

Voltage regulation by the PV inverter can be implemented with the OpenDSS function shown in Figure 27 by creating a curve with a very steep slope around the desired voltage setpoint. With the steep slope, the solar inverter will deliver whatever reactive power is necessary to regulate the voltage until the inverter rating is reached. The results for the daily profile of voltage at the PCC for each of the three solar scenarios are compared to the basecase without PV in Figure 28.

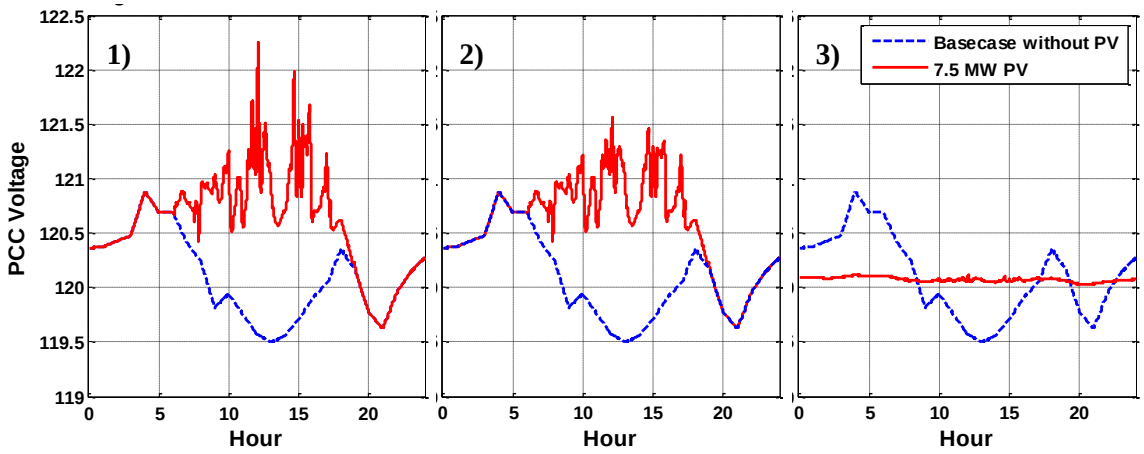


Figure 28. PCC voltage for each of the three solar scenario: 1) unity power factor, 2) volt/var control with deadband, and 3) voltage regulation.

For the voltage regulation case, a significant amount of reactive power is required. The reactive power output is shown in Figure 29. In this simulation the inverter rating was never reached (because of the low solar output on this cloudy day), so the exact number of required vars was always able to be generated or absorbed to regulate the voltage. Under extreme conditions of high solar power output (kW) or large voltage deviations, the PV inverter can reach the rating limit and would not be able to fully regulate the voltage. The solar inverter must stay within its kVA rating, so an inverter rated for the PV system would have very little capacity left for producing or absorbing Vars under high solar output weather conditions. This headroom for reactive power

output between the inverter rating and the real power solar output varies throughout the day as the solar irradiance varies. If the inverter control (fixed power factor, schedule, or function) requests a higher reactive power output than the available headroom of the inverter kVA rating, either the reactive power or the real power must be reduced from the specified conditions.

Using reactive power output from PV inverters also impacts the power factor of the line flows in the distribution system. For example, with high penetrations of PV, a significant portion of the real power of the feeder could be generated by the PV. On the other hand, the PV may be absorbing large amounts of reactive power to decrease the system voltages. PV would be decreasing the real power flowing through the substation transformer and increasing the reactive power flow, making the power factor go towards zero. The same impact would be true for the power factor of the current flowing through distribution system lines and relays. Moving more reactive power around the feeder can also increase system losses.

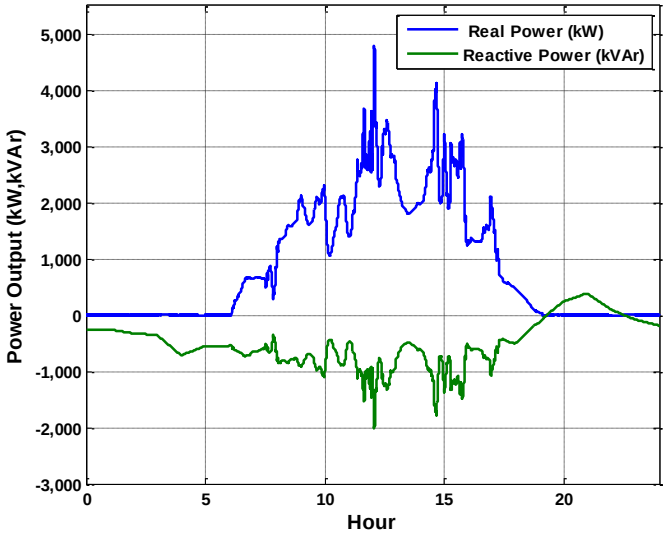


Figure 29. PV plant power output using voltage regulation control on 4/20/11.

With increasing penetrations of solar on the distribution system, reactive power capabilities of inverters can be used to support voltage and mitigate any over voltage conditions caused by real power output. Detailed timeseries analysis was shown to

demonstrate the exact impact of PV output power factor and reactive power on the distribution system voltage. Additionally, two methods are shown for controlling over-voltage conditions using a power factor schedule and a power factor function. Two forms of voltage regulation using volt/var inverter control were also shown. The expansion of PV and distributed generation to high penetrations on the distribution system requires intelligent and well controlled devices to ensure reliable service and minimal impact to the existing customers.

3.6 Voltage Regulator PV Impact Simulations

The interaction between solar variability and the distribution voltage regulation equipment is a serious concern to the utility. Voltage regulators have many different control modes and settings that can be selected by the distribution engineer when they are installed. In this section the PV irradiance variability profile impact on the number of tap change operations is investigated. In addition, several different voltage regulator control modes are implemented and simulated to determine the different interaction with PV.

3.6.1 Impact of PV Variability Profile

Since changes in PV power output can create tap changes in distribution system voltage regulation equipment, it is expected that higher amounts of solar variability will have a more significant impact to the number of tap changes. The solar variability is determined by the weather, cloud structures, and cloud speed. Each of these factors are geographically dependent, and specific locations will have higher solar variability than others. In this section, high-resolution solar data is used from ten different locations in order to study the impact of different variability profiles.

In order to quantify the variability of each location, a metric was developed in [132] that creates a VS_{cdf} based on the analysis of the 30-second ramp rates. The VS_{cdf}

value was determined for the entire dataset at each location and is shown in Figure 30. For the distribution simulations for each location, a sample week of irradiance data was chosen that best matches the VS_{cdf} for the entire dataset. The irradiance at each location was scaled to represent a 3MW central PV power plant. This was done by: (1) smoothing the irradiance to represent the average irradiance over a 3MW plant footprint (~18.5 acres) using the wavelet variability model [123] and (2) converting the irradiance to power output of a 3MW PV plant using a simple linear irradiance to power model with clipping at 3MWs. The weekly power output samples at each location are shown in Figure 31. Consistent with their low VS_{cdf} values, Las Vegas, Livermore, and Sacramento all had multiple clear days in their weekly samples. Conversely, Lanai, Oahu, and Mayaguez, all locations with high VS_{cdf} values, had many highly variable days in their sample weeks.

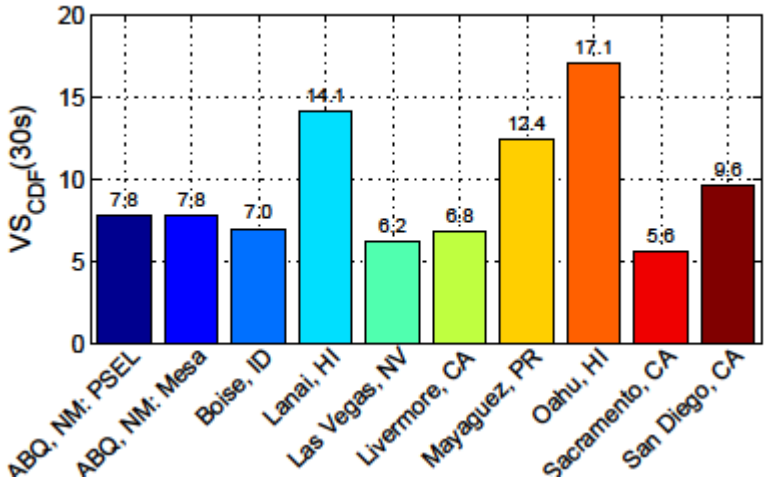


Figure 30. Bar chart of the 30-second VScdf values at each location.

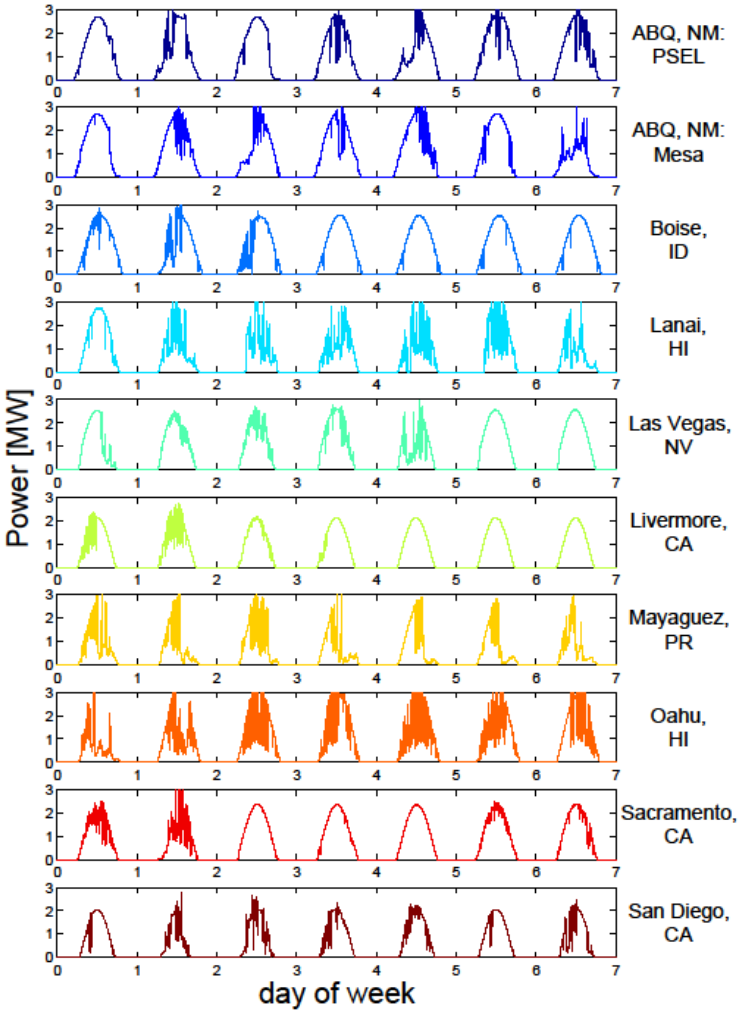


Figure 31. Sample weeks for distribution studies.

The agricultural feeder shown in Figure 32 was used for all simulations. One distribution system was used so that the results can be better correlated to the single variable of PV variability profiles changing. This feeder was chosen partly because of the location of its voltage regulator (approximately halfway down the feeder), which allowed for simulation of a 3MW PV plant just beyond the voltage regulator. For all simulations, a consistent load profile from the peak load week was used. QSTS power flow analyses at 1-second resolution were computed through OpenDSS coupled with MATLAB [121]. This analysis was run 11 different times: once with no PV as a base case, and once for each of the 10 different PV power profiles.

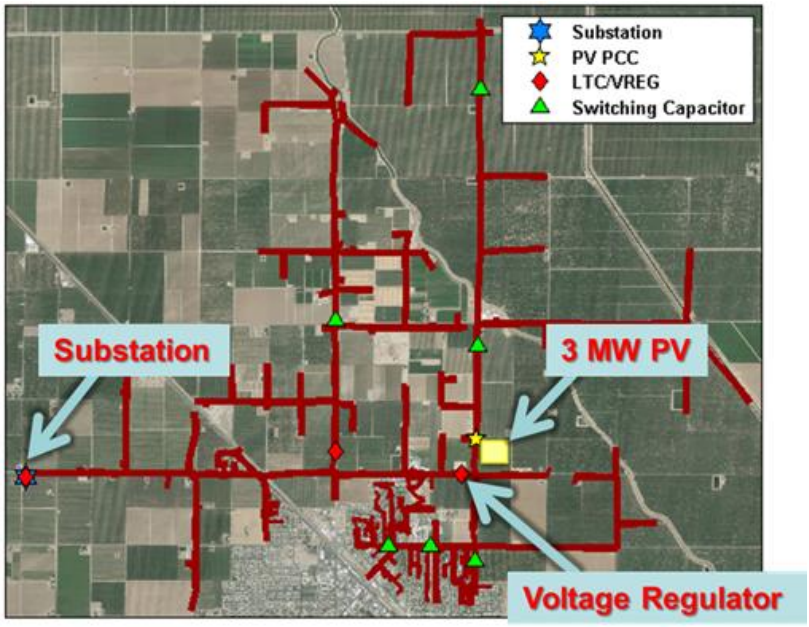


Figure 32. Layout of the study distribution feeder showing the location of the substation, voltage regulator, and 3 MW PV.

An example of the results for the QSTS analysis of the base case and the Lanai PV power profile are shown in Figure 33. The power through the voltage regulator in the base case is the load profile. The week starts on a Sunday (hours 0-24) and ends on a Saturday (hours 144-168), and both of these weekend days have lower load than during the weekdays. Since voltage regulators are installed to regulate the voltage variations caused by the load, there can be a significant amount of tap change operations even without PV. Over the whole week, there were 78 tap change operations in the base case. When using the Lanai PV power profile, the power through the regulator fluctuates much more than in the no PV case. On the Sunday (hours 0-24), the Lanai power profile was mostly clear, and there is almost no increase in tap change operations over the base case. On the Friday (hours 120-144), however, there was an especially large increase in the number of tap change operations compared to the base case. The irradiance profile on this day was highly variable during a time of relatively low load, leading to more voltage fluctuations. Over the entire week, there were 190 total tap change operations, more than double the number of operations as the base case. This increase in tap change operations

may lead to increased grid operation costs if the tap changers need to be replaced sooner than they would without such PV variability.

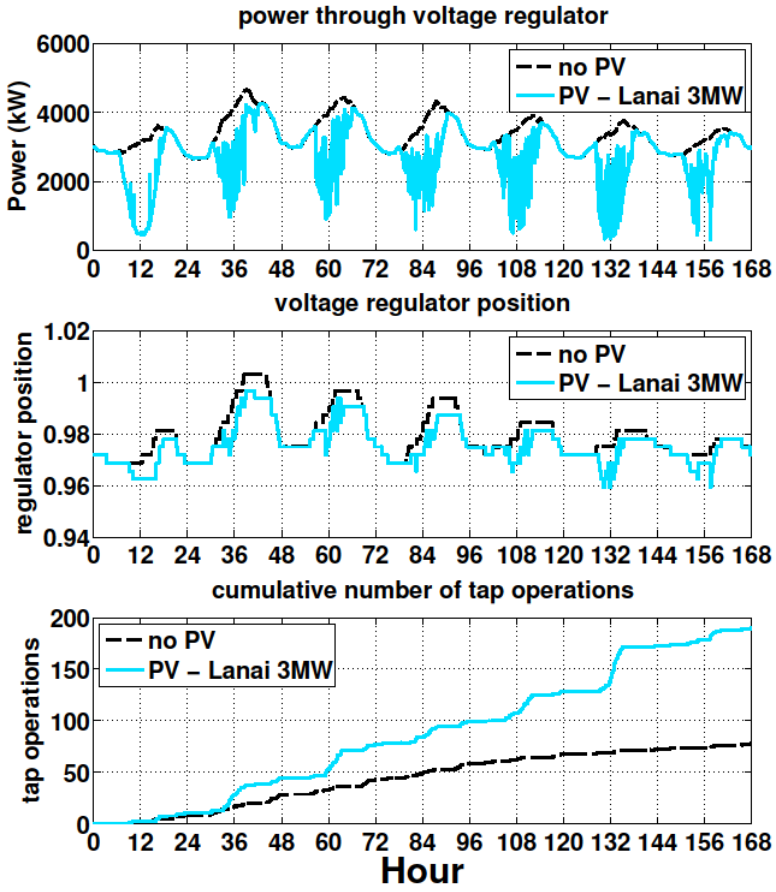


Figure 33. Power through voltage regulator (top), voltage regulator position (middle), and cumulative number of tap changes (bottom) for the feeder base case with no PV (black) and for the 3 MW Lanai test case (light blue).

Figure 34 shows the percent increase in the number of tap operations in the sample week for each of the PV power profiles compared to the base case. The Boise and Livermore locations resulted in no increase in tap change operations over the base case. This is not to say that the PV variability had no impact on the tap change operations. The tap position timeseries was not identical between the base case and either the Boise or Livermore simulations, even though the cumulative number of tap changes was the same. The PV variability at times damped some of the load variability, leading to reduced tap

operations, and at other times augmented the load variability and increased tap operations.

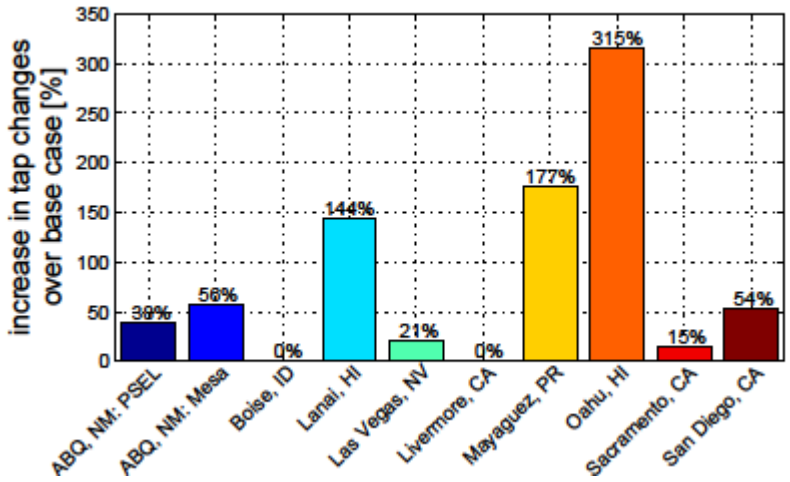


Figure 34. Percent increase in tap changes over the base case with no PV during the sample weeks when using a 3 MW PV variability profile from each location.

The distribution simulations results using different PV variability profiles by location have strong implications for distribution studies and PV integration. Significant overestimation or underestimation of the impact of PV can occur due to choosing an inappropriate solar variability profile. For example, a distribution study that used the Oahu PV profile to represent a feeder in Livermore would overestimate the number of tap changes by over 300%. Such a study might erroneously assign a high cost to PV integration due to increased tap changer maintenance. Conversely, a study of a distribution feeder in Oahu using PV data from Livermore would significantly underestimate the impact on tap change operations, and may lead to equipment failing much sooner than expected.

QSTS 1-second resolution simulations were performed for a 3 MW PV interconnection with different PV variability profiles. Depending on the variability of each location, there is a significant range of increase in the number of voltage regulator tap changes during the week simulations.

3.6.2 Voltage Regulator Control Modes

While the previous section focused on the solar irradiance input of the interaction between PV variability and voltage regulators, this section studies the variations caused by different voltage regulator control settings. The most basic voltage regulation devices include a voltage set point, a voltage bandwidth, and a time delay. Another common control setting may be the use of Line Drop Compensation (LDC). LDC allows for the setting of a voltage control point other than at the location of the LTC or VREG by programming estimated real and reactive impedances to the desired point and then monitoring the measured current in that direction to estimate voltage drop [73]. Most modern LTC/VREG controls offer several modes of operation, such as sequential, time integrating, and voltage averaging [133]. Sequential mode of operation is the most common and is sometimes the default time delay control mode. During the time-out period in sequential mode, the voltage is continually sampled at a sub-second rate. If during the time-out the voltage returns to a level within the bandwidth, the timer is reset. If the voltage remains out of band for the duration of the time delay setting, an appropriate tap change is activated [133]. There are also settings designed to offer flexibility of control during reverse power, such as bi-directional and cogeneration modes. Bi-directional modes simply implement a separate set of control parameters when in reverse power. Cogeneration modes can offer the ability to focus the voltage regulation on a certain point, such as a cogeneration interconnection point, regardless of the power direction. These control options can make a difference in the way PV affects voltage regulation switching operations; therefore, it is important that the correct control settings be determined and properly implemented in the simulation software.

Using the same simulation setup from the previous section, a few other regulator control parameters are studied for their impact on the number of regulator tap changes. The same 1-week simulation at 1-second resolution is performed for eight irradiance

locations, and for each simulation, the number of voltage regulator tap changes is recorded. One of the most common settings (and most likely to be modified) is the time delay on the regulator. In Figure 35, the regulator delay is changed to be 30, 45, and 60 seconds. As expected, the longer delay times have fewer number of tap changes because the regulators take a longer time to respond to the solar variability. For locations like Livermore with little solar variability, modifying the regulator delay had little impact. Conversely, for Oahu, doubling the delay from 30 seconds to 60 seconds changed the increase in tap changes from 379% increase to a 238% increase.

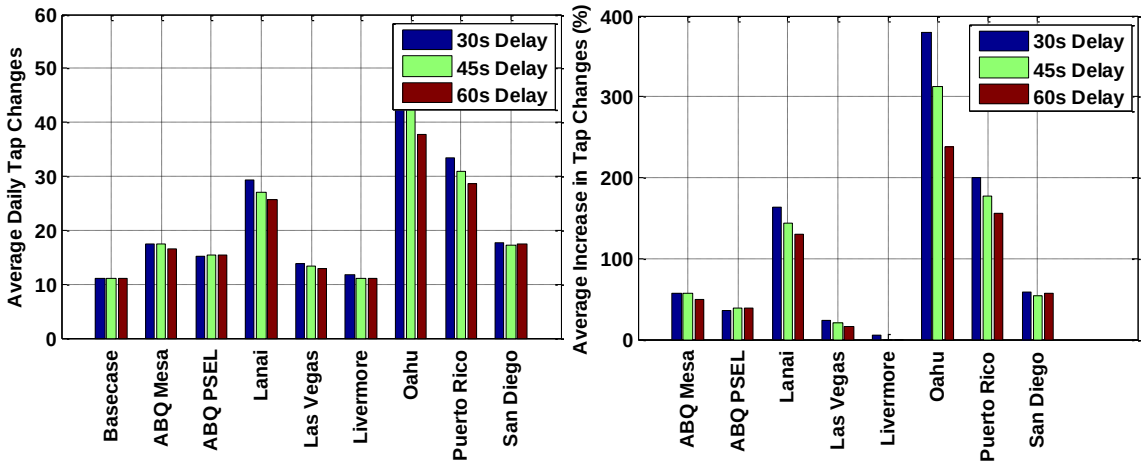


Figure 35. Change in tap changes as a function of regulator tap delay and variability location profile.

Voltage regulation devices have evolved over time to provide increasingly complex and customized control modes for many different applications. It is unlikely to find distribution system analysis software that is capable of QSTS and offers the ability to simulate all existing control modes. However, if the QSTS software offers COM interface capability, it is possible to develop and implement control algorithms through an external program [68]. For example, OpenDSS is cable of QSTS, but it only offers a simple control algorithm for voltage regulators and LTCs that initiates the time delay with the first instance of an out of band voltage, then disregarding the voltage during the time delay, it simply checks the voltage at the end of the time delay and reacts according to

whether the voltage is still out of band at that point. This type of control in OpenDSS is different than the common sequential control, time integrating, or voltage averaging. PV power output can be highly variable under cloudy sky conditions, potentially causing voltage variations that could be missed during the time delay in OpenDSS.

Using the COM interface in OpenDSS, it is possible to implement more realistic control modes using programmable software, such as MATLAB. OpenDSS is used to solve the power flow, and the control logic is implemented in MATLAB to monitor the voltages and currents and control devices according to a customized algorithm. An example of the interfacing process for controlling a substation LTC is shown in Figure 36. For each time step in the OpenDSS time-series power flow solution, MATLAB reads the transformer voltages and currents through the COM interface. MATLAB calculates the control voltage based on transformer voltage and the PT ratio, as well as the transformer current, CT rating, and LDC X and R settings if an LDC is present.

If the calculated control voltage is out of band, the custom control logic block is entered. The custom control logic block can be customized, from simple delays to more complex controls and secondary checks, such as remembering when the most recent tap change occurred. When all conditions are met, MATLAB commands the appropriate winding in OpenDSS to move to the new tap position.

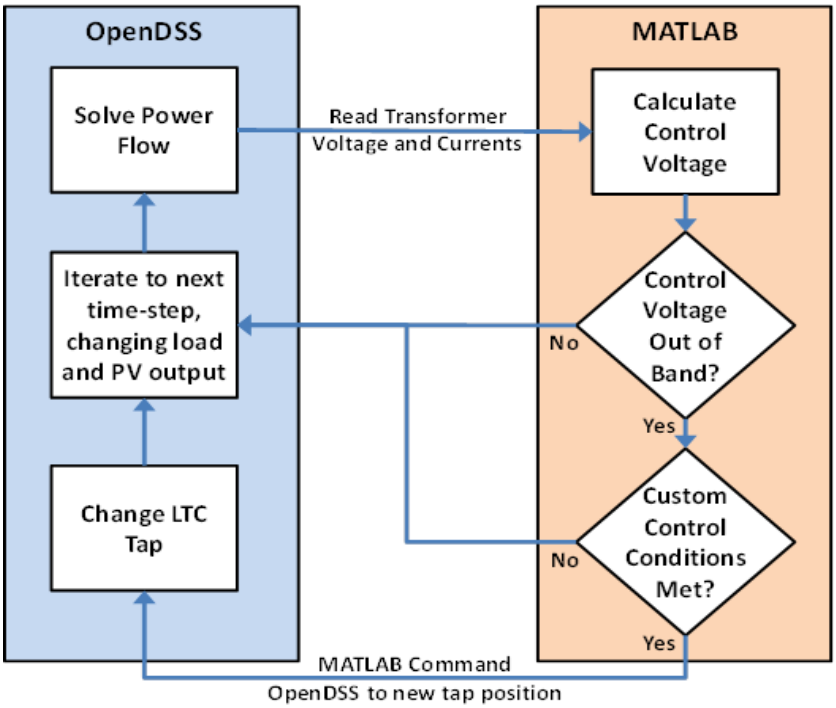


Figure 36. MATLAB/OpenDSS interfacing for custom LTC control.

Figure 37 provides a visual example of the potential difference that can occur between a simple control algorithm and the sequential mode, which properly simulates time resets when the voltage returns in band. For both control modes shown, the voltage setpoint was 124V, the bandwidth was 2V, and the time delay was 60 seconds. The OpenDSS default control mode results in a tap change at 1:25:10 PM simply because the voltage is out of band when the initial counter expires. The sequential control mode does not result in a tap change here because the time delay was reset when the voltage surged back within band, resetting the delay. This illustrates a situation where properly modeling the actual control mode can make a difference.

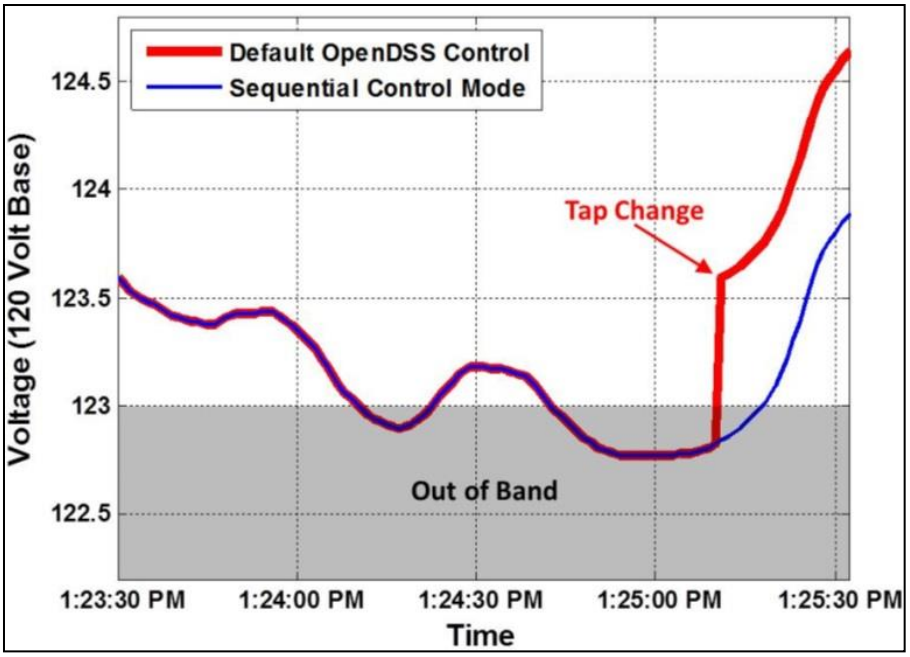


Figure 37. Control mode simulation comparison.

The method of MATLAB controlling the LTC in an OpenDSS simulation is demonstrated for a 9-month simulation of the feeder in Figure 38. The QSTS simulation was performed at one-second resolution using time coincident load and irradiance data. A 7.5 MW PV system was simulated at the end of the feeder, representing 100% penetration of the feeder annual peak load. A base case without PV and the PV case were run utilizing both the default control mode in OpenDSS and the customized sequential mode using MATLAB. The use of external MATLAB control of the LTC was validated in both the base case and the PV case by implementing the default OpenDSS control algorithm through MATLAB and comparing it to the results obtained in OpenDSS alone. Identical results were obtained for the LTC taps and number of operations for the simulation period. Figure 39 shows a plot of the LTC activity for the 9-month simulation with PV using a sequential control mode algorithm through MATLAB.

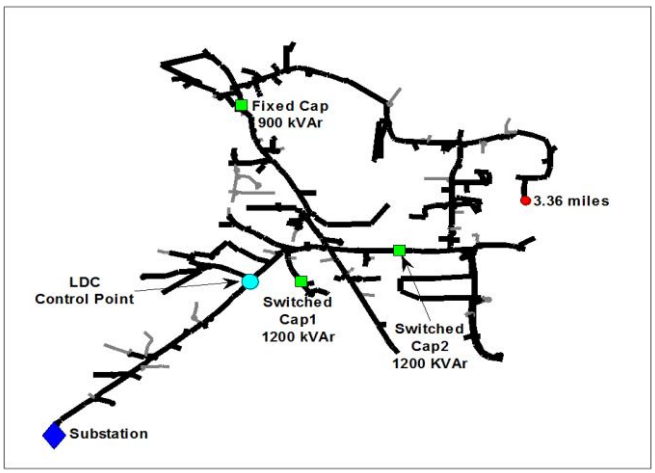


Figure 38. Feeder A topographic layout.

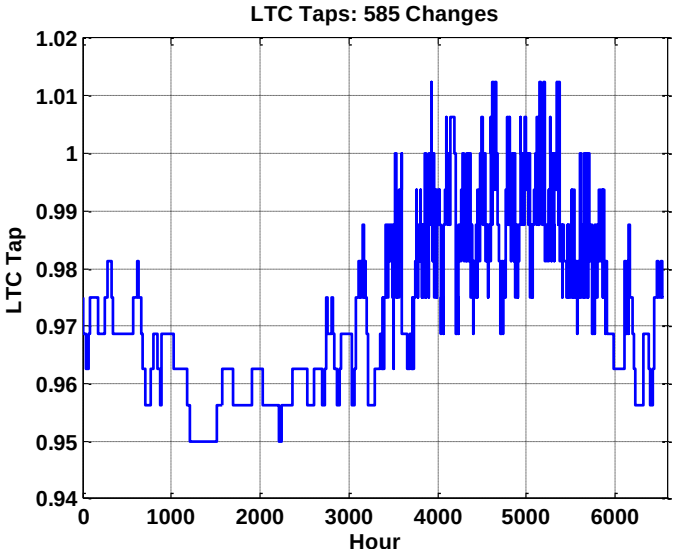


Figure 39. LTC tap position controlled by MATLAB using sequential control mode during the 9-month simulation with 7.5 MW PV.

In this example, there were no differences in operation totals for the LTC found in either the base case or the case with PV when using the sequential control algorithm through MATLAB. Conceptually, an LTC connected to a large transformer and stiff transmission source serving several feeders is less likely to be affected by PV and/or load variations during voltage regulation device time delay counters as a line voltage regulator or capacitor bank out on a feeder near a PV system, where voltage fluctuations are much greater. For the PV scenario, it was expected that the control mode would affect the

number of operations during the simulation because of the high resolution variability. The results show that the control mode had no impact, mostly due to the fact that the PV penetration was 100% of the feeder load but less than 20% of the total substation load through the LTC.

There are many factors that need to be properly simulated in order to obtain valuable results from an interconnection study on voltage regulation device operations using QSTS simulation. First, the range in the increase of tap changes due to PV variability was shown for ten different locations. Second, the regulator control time delay was increased to mitigate the large increase in number of tap changes due to highly variable PV output. Third, it was shown that you can implement complex voltage control algorithms through MATLAB to improve the accuracy of the results.

3.7 PV-Induced Low Voltage and Mitigation Options

This section describes the phenomena of low voltages on a feeder that are caused by the combination of PV and line-drop compensation (LDC). ANSI C84.1 [134] defines the steady-state voltage range that must be maintained for any 10-minute average. For low voltages, the ANSI threshold of 117 V (for systems above 600V) is applied to the primary system buses, and the threshold of 114 V (for systems below 600V) is applied to the secondary system buses. Voltages below these threshold, or under-voltages, are generally only caused by PV when the feeder voltage regulation contains an LDC. LDC is a voltage regulator setting that virtually sets the voltage control point downstream of the location of the LTC/VREG. This is typically done by providing impedance characteristics, both real and reactive, that are representative of the section of feeder between the LTC/VREG and the virtual control point. The control then takes the impedance and the line current into account and adjusts taps accordingly. LDC can be useful in cases where optimal VREG locations present excessive physical obstacles.

Other applications of LDC include conservation voltage reduction (CVR) and dynamic regulation for extreme load conditions.

Because the LDC assumes a certain voltage drop on the feeder for a particular current drawn, the PV generation effectively tricks the LDC into believing there is less voltage drop on the feeder because the current decreased. This is mostly commonly an issue when PV is near the voltage regulator equipment with LDC causing under-voltages toward the end of the feeder. PV proximity to the regulator plays a role in the risk of under-voltages. The further the PV is from the LTC/VREG, the more likely it is to counteract the under-compensation with the natural voltage rise inherent to PV. In fact, over-voltages are still possible when large enough PV is connected to a regulator with LDC. Figure 40 shows simulation results of Ckt24 [135] to show the voltage profiles of a feeder with LDC as the PV location varies. Ckt24 is a 34.5 kV feeder with a 28 MW peak load. The substation 230/34.5 kV transformer has an LTC with LDC. The LTC setpoint is 123 V with LDC of R=7 V and X=0 V (volts at rated CT current). Figure 40 illustrates an example of how under- and over- voltages can exist on the same feeder with LDC depending on the location of PV.

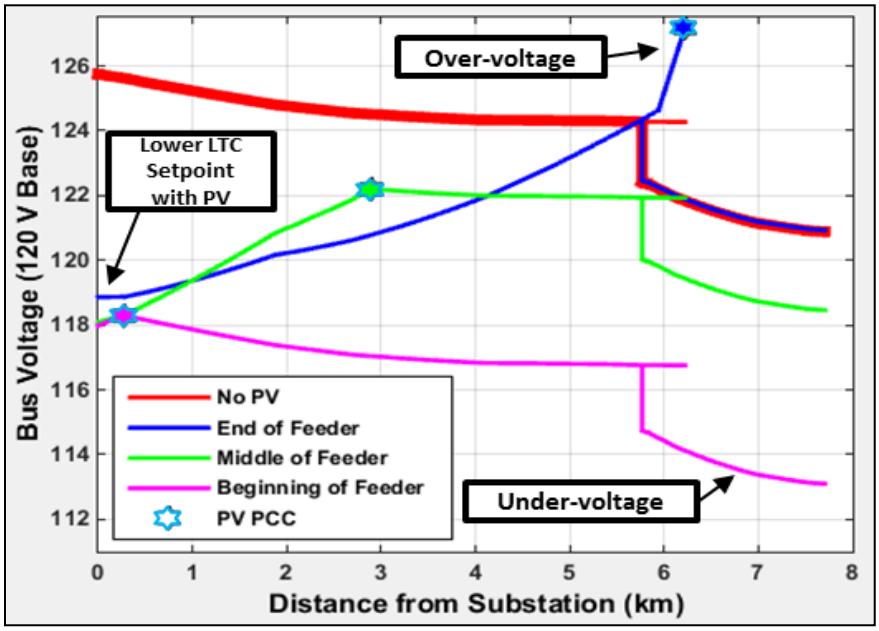


Figure 40. Ckt24 voltage profiles for basecase and with PV near beginning, middle, and end of feeder with LDC on the LTC.

Using the method described in [136, 137] and Chapter 5, the maximum PV sizes that can be placed at each bus before a violation occurs is determined. Figure 41 shows the maximum PV interconnection size for buses along the main backbone (94 locations) along with the violation type that was first an issue. The limiting factor near the substation is under-voltage, thermal line loading in the middle, and over-voltage at the end. In the cases where under-voltage is the limiting factor, the under-voltage never occurs at the location of PV.

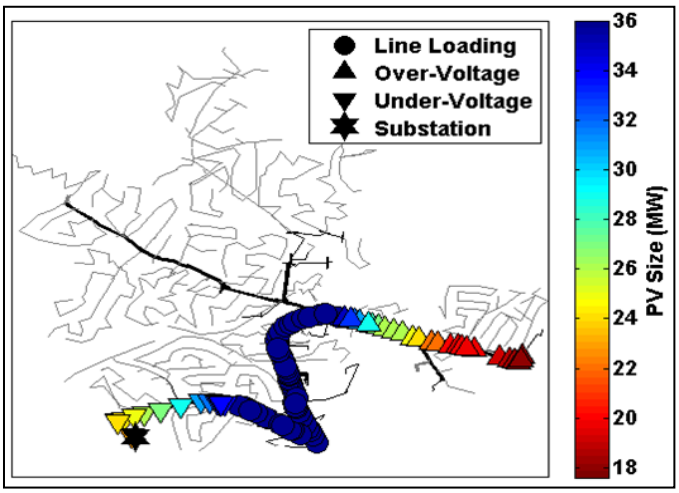


Figure 41. Ckt24 topography and locational hosting capacity along backbone of interest.

The distribution of the limiting factors on the Ckt24 backbone could commonly be expected for feeders with LDC enabled. In order to relieve the voltage issues shown, two potential mitigation strategies are studied. First, adding smart inverter functionality, specifically Volt/VAr control, is investigated. Second, removing the LDC control logic from the substation LTC is considered. Figure 42 shows the hosting capacity vs. distance for three cases: PV with LDC, PV with Volt/VAr control, and PV with LDC removed. A standard Volt/VAr curve algorithm was used assuming enough AC capacity to never curtail the real power.

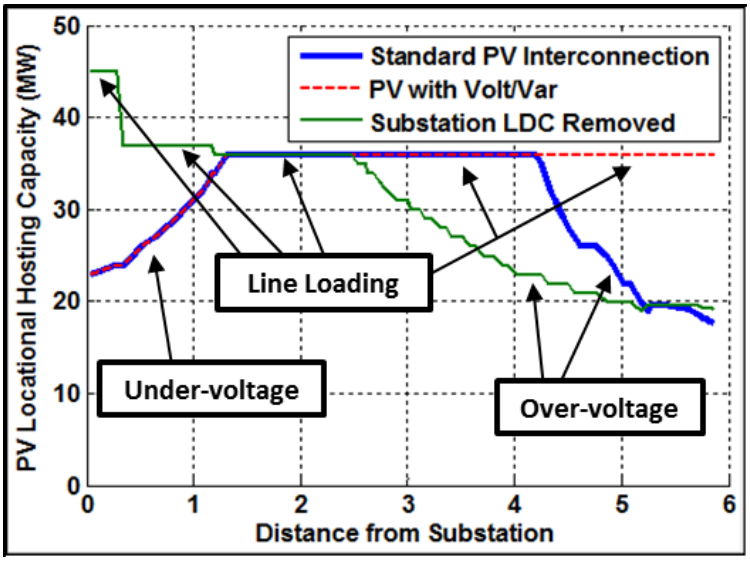


Figure 42. Ckt24 hosting capacities for standard PV with LDC, PV with Volt/VAr control, and standard PV with LDC removed.

The blue line in Figure 42 reflects what was observed in Figure 41. The red line demonstrates that simply adding Volt/VAr control to the PV simulations does not eliminate under-voltages at the end of the feeder caused by placing the PV near the LTC with LDC. Volt/VAr does eliminate all over-voltages caused by the PV when it is at the end of the feeder. Eliminating LDC and raising the LTC setpoint just enough to raise all voltages to within compliance at peak load (green line) clearly eliminates the under-voltages issues, but not having an LDC causes more over-voltage constraints further out on the feeder because the LTC is not dropping the setpoint with increases in PV size.

The previous example demonstrated under-voltage violations on the feeder with PV when PV is placed close to a regulator with LDC. The second example demonstrates how a substation transformer with LDC that serves multiple feeders can interact with PV on one feeder to create low voltages on a separate feeder. For this example, the 12.47 kV feeder UQ12 with a 6.2 MW peak load is used. The substation 69/14 kV transformer has an LTC with LDC. The LTC setpoint is 121 V with LDC of R=5 V and X=3 V. There are no VREGs and four fixed capacitors totaling 1.8 MVAr. The general topology of the feeder and simulated PV scenario is shown in Figure 43.

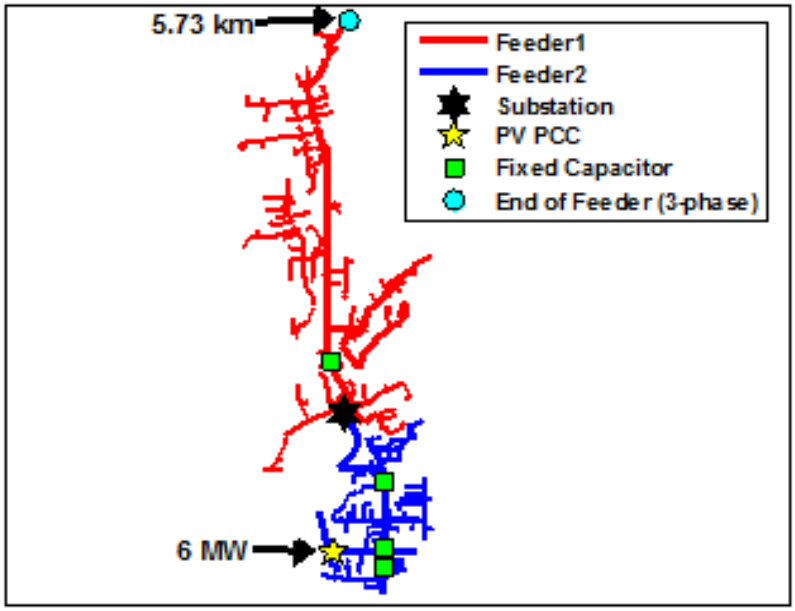


Figure 43. UQ12 topography and PV **location**.

UQ12 was chosen because it essentially splits into two feeders just outside the substation, as shown by colors in Figure 43. As shown in Figure 44, PV voltage rise may offset LDC under-compensation on the feeder with PV, depending on location and magnitude. On the other hand, LDC under-compensation affects other feeders regardless of PV scenario. Figure 44 shows the voltage profiles of both "feeders" of UQ12, for the basecase (solid lines) and the case with 6 MW of PV at the end of Feeder 2 (dotted lines). This shows a PV scenario that offsets the LDC under-compensation on the feeder with PV, but under-voltage on the other feeder, which would be unchanged regardless of PV location on Feeder 2.

These examples demonstrate how detailed analysis is necessary to detect potential under-voltage issues caused by PV, which generally occur far from the PV location. It is most commonly thought that PV causes high voltages, but under circumstances with load drop compensation, low voltages can also occur. For any voltage issue, the ANSI standard applies to a 10-minute average, which means QSTS must be used to detect any violations.

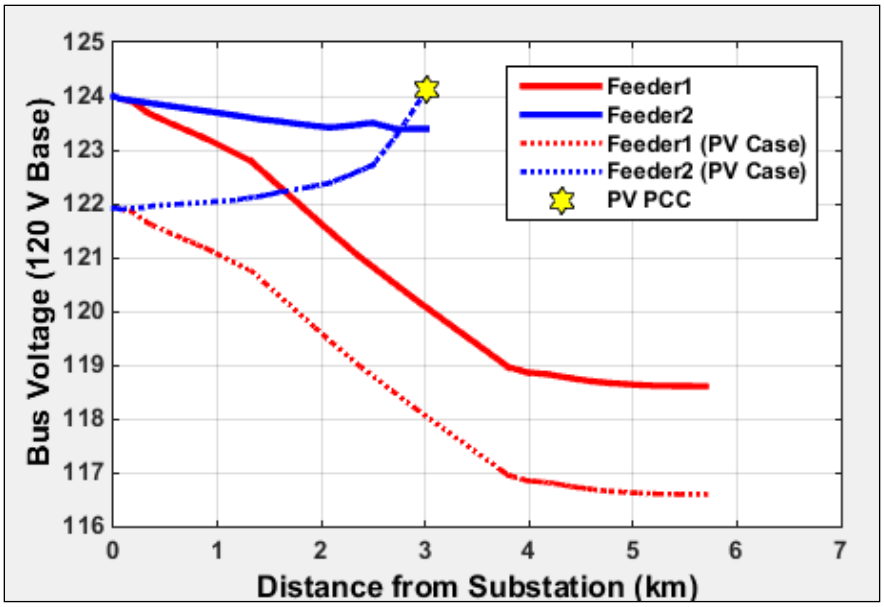


Figure 44. Feeders 1 and 2 voltage profiles, with and without PV.

3.8 Improved Computational Speed for Analyzing the Impact of PV Variability and Ramping Events on Distribution Voltage Regulation Equipment

Finally, new methods are developed to improve the simulation speed of time-series simulations for more efficient PV interconnection screening. The time-variant nature of photovoltaic (PV) systems can negatively impact the distribution system with voltages exceeding operational limits due to ramps in PV output (short-term variability) as well as increased regulator tap changes from daily changes in PV output (long-term variability). Two new methods that avoid performing computationally intensive and cumbersome time-series simulations are created for studying these variability impacts: extreme power ramps on voltage and variability on number of tap changes.

As the penetration of PV increases on the distribution system, there is rising concern about the interaction between PV variability and on-load tap changers (OLTC) or voltage regulators. The impact to the electric grid depends on the frequency, magnitude, and timescale of the PV variability. Very fast PV power output ramps can cause voltage

flicker and extreme voltages due to their speed and magnitude before the voltage equipment acts to bring the voltage back into range. Additionally, frequent fluctuations in the PV output can create a large increase in the number of tap changes over a period of time, prematurely wearing out the existing infrastructure [75]. A standardized method is needed to manage PV interconnection request in a faster way that would not require time-series power flow solutions but would be able to study all potential issues from PV variability interacting with voltage regulation equipment.

In this section, the impact of PV variability on voltage regulation equipment is separated into two categories: short-term variability and long-term variability. The short-term variability can occur faster than the voltage regulation equipment, such as on-load tap changer (OLTC), can react, which causes extreme transient voltages during the PV ramp. The long-term variability increases the number of total tap changes, leading to quicker degradation of equipment. Methods are developed for analyzing the impact of both short-term and long-term PV variability on the distribution system quickly and efficiently for interconnection screening.

3.8.1 Short-Term Variability – Extreme Ramp Analysis

Short-term, very fast solar variability can occur on timescales faster than regulation equipment normally acts on a distribution system. Most OLTCs have a delay of 30 to 90 seconds between detecting voltage issues and taking corrective action. This is part of the distribution system design to reduce the number of unnecessary tap changes. Solar irradiance has been shown to have variability and high ramp rates, even in the range of a few seconds. While, the size of the geographical footprint of the PV plant can smooth the expected power output variability compared to a point irradiance sensor [138], [139], the power output can still ramp many megawatts in a minute under extreme cases.

The extreme ramps in PV output can cause voltage issues before the end of the time delay on the voltage regulation equipment. Under normal operation, when the voltage begins to deviate from the expected range, the voltage regulation equipment can respond and correct the voltage. During cloud transients, the ramp in PV power output can quickly raise the voltage before the regulator tap change.

To determine the expected change in PV output, 1-minute ramp rates of existing PV systems can be studied. These ramp rates are at the timescale of the OLTC delays, and an analysis of the worst case scenario with the highest ramp rates (top 0.1% of 1-minute ramps) will provide a reasonable comparison for the most extreme PV ramp size within the delay window. Literature shows that a 32 MW plant can ramp more than 10.56 MW, and a 24.5 MW plant can ramp 8.58 MW [140]. Similarly, an 80 MW plant can ramp more than 14.4 MW in a minute [140]. From this, it is assumed that a large plant (>20 MW) can ramp approximately 10 MW during the delay window. For smaller plants, the per-unit ramp rates are higher, but the ramp in MW/min is smaller. Small systems generally have 99.9% of their ramp rates under 50% of capacity, but the worst ramp can be close to 70%. A 5 MW system [140], a 4.5 MW system [140], 13.2 MW system [141], and three systems greater than 10 MW [142] all have 50% capacity 1-minute ramp rates at 99.9% on the ramp distribution cumulative distribution function.

The PV ramp analysis is performed on Feeder J1, which is an actual 12.47 kV distribution system with the model publically available online [143]. For voltage regulation, the feeder has an OLTC at the substation and three sets of voltage regulators along the feeder. There are also five capacitor banks on the feeder. The peak load of the feeder is around 6 MW. The topology of the feeder can be seen in Figure 45 and Figure 47. The 3-phase unbalanced distribution system is simulated in OpenDSS controlled by MATLAB [117], [121].

A large utility-scale PV system rated at 3MW is simulated interconnected at the location shown in Figure 45. A realistic ramp is simulated using 1-second irradiance data

measured in California. The irradiance data was transformed to power output with the appropriate geographic smoothing for the land area covered by a 3MW plant using the Wavelet-Based Variability Model (WVM) proposed in [123]. The most extreme power output ramp is shown in Figure 46A where the system ramps 1.1 MW in 30 seconds and 1.4 MW in a minute. This ramp rate corresponds well with the 1-minute ramp rates found in literature discussed in the previous section.

The high speed fluctuations in PV power output are simulated using detailed 1-second quasi-static time-series (QSTS) power flow analysis [73] to model the voltages and control actions of the voltage regulation equipment [68]. The voltage at the point of common coupling (PCC) for the PV system is shown in Figure 46B. The feeder voltage regulators appropriately change taps at the end of their delay to bring the voltage back within range. There is however, a period of about 30 seconds where the voltage exceeds the ANSI C84.1 limit of 1.05 pu voltage [134]. While the ANSI range is defined for the 10-minute average voltage and does not apply to temporary voltage excursions, this temporary overvoltages could cause other problems like the PV inverter tripping off [144] or damaging customer equipment if the voltage is significantly high [145],[146].

The feeder voltages before and after the regulator changing taps are shown in Figure 45. In both cases, the PV power output is approximately at the full rated output of 3MW. This demonstrates how much higher feeder voltage can be during a ramp, solely due to the interaction between the PV variability and the regulation equipment delays. Similar analysis can be done for the down ramps in PV output during sudden cloud cover that could cause transient low voltage issues [147].

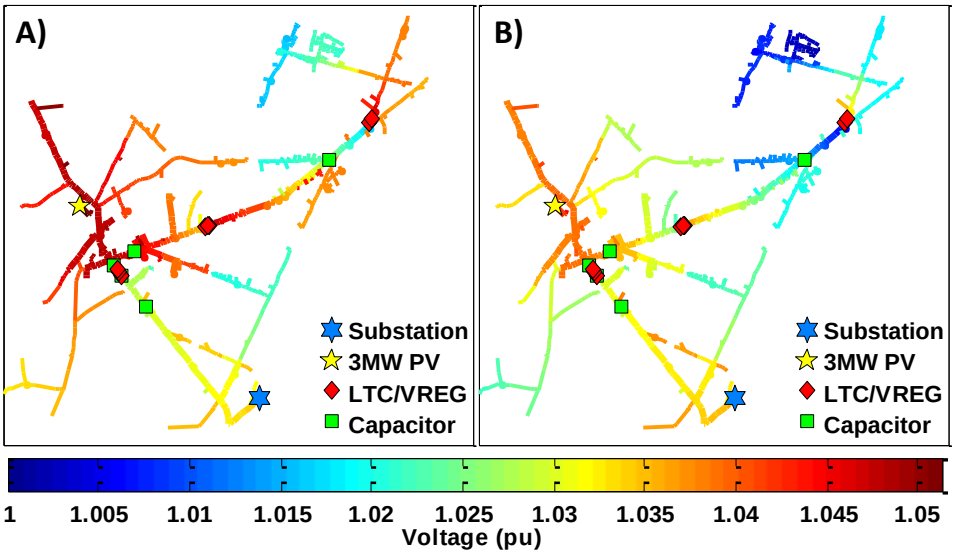


Figure 45. Voltages on the feeder while the PV system is outputting 3MW A) during the PV ramp up before the regulation equipment reacts, and B) in steady-state.

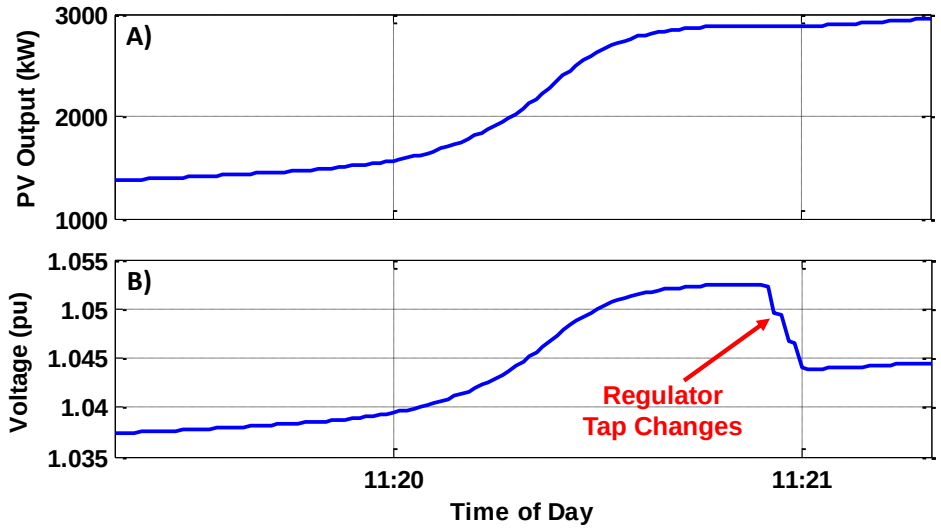


Figure 46. Extreme ramp up in power output for a 3 MW PV system after a cloud with A) the PV power output and B) the feeder voltage at the PV system medium-voltage side of the interconnection transformer.

While detailed QSTS simulations provide insight into the interaction between PV and the voltage regulation equipment, performing many of these time-series simulations for the entire ramping scenario at high resolution can be very computationally intensive. This is especially an issue if it is desired to simulate the entire PV output profile for a year to determine if any of the ramps will cause voltage violations.

A faster method is presented here using only two power flow simulations for a PV output up-ramp, and two power flow simulations for a PV down-ramp. The improved simulation speed is achieved by locking the voltage regulation equipment after the first power flow and simulating the maximum possible PV change before the voltage regulation equipment will take the control action.

To simulate the worst case ramp at the top 0.1% of 1-minute ramps, a simple formula for the worst-case ramp magnitude is established from the previous literature. For PV systems under 20 MW, a 50% ramp magnitude is studied. For larger systems greater than 20 MW, a 10 MW ramp magnitude is used in the simulation. If local high resolution data is available, or it is known that the variability is significantly different for certain climate conditions, the 50% ramp rate could be varied for the interconnection location. For the up ramp, the appropriate ramp magnitude is subtracted from the PV power output, and OpenDSS is used to solve for the state of the voltage regulation equipment at the smaller PV output. The voltage regulation equipment is then locked and the PV output is increased to full output. The down ramps are studied using a similar method of locking the voltage regulation equipment at full PV output and decreasing the PV size by the ramp magnitude. This allows for easy impact studies without long time series simulations or requiring high resolution irradiance data.

This proposed method is similar to the "voltage change" test that locks the distribution equipment without the PV and then adds the full rated output of the PV system into the circuit [84],[145]. The voltage change test limits how much the distribution system voltages can deviate during a full switch from off to on. The proposed PV ramp simulation method is different in that it is not focused on the change in voltage, but is identifying any temporary overvoltages that occur. Under normal operation, PV systems do not change between full output and zero output during the regulation equipment delay time. The proposed ramp method tests more realistic PV ramp magnitudes for any temporary overvoltage conditions.

The methodology is demonstrated on the example feeder. Figure 47a depicts the results of a steady-state solve with the PV outputting rated power and the voltage regulation equipment allowed to act freely. In Figure 47b the down ramp is simulated by locking the regulation equipment, and the PV system is then set to output half of its rated power (if the PV system's rating is above 10MW, then the output is rated power minus 10MW).

Figure 47c shows the steady-state solution with the regulation equipment allowed to act freely and the PV system still outputting half its rated power. Permitting the voltage regulation to freely act allows the voltage profile to return to a state more similar to those shown in Figure 47a. Figure 47d contains the simulation for a PV output up ramp with the regulation equipment locked and the PV system outputting rated power. This up-ramp simulation results in the most extreme high voltages of the 4 modes.

The simulations in Figure 47 show the necessity of considering PV ramps for interconnection studies. A simple steady-state power flow solution would show the voltages in Figure 47a and Figure 47c, but the most extreme voltages (high and low) are caused by PV ramps within the delay window.

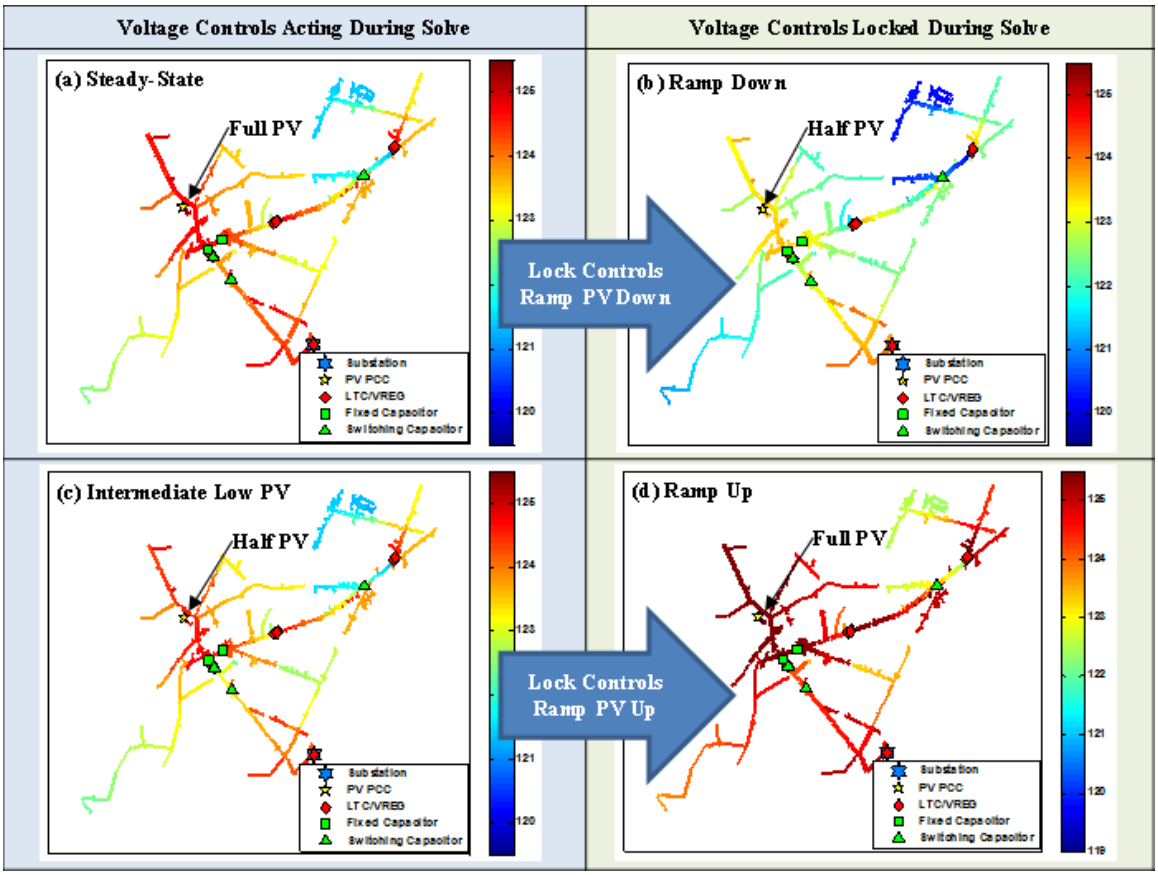


Figure 47. Circuit plots for J1 at full load contoured by bus voltage (120V-base) with a 2.5MW PV system and voltage regulation at the top of their bands shown for the 4 different solve modes: a) Steady-state b) PV down ramp c) PV steady-state before up ramp d) PV up ramp

The ramp simulation method only requires four power flow solutions, compared to around a hundred power flow solutions for a single ramp timeseries or millions of power flow solutions for the PV ramps for a year. The improved ramp simulation method quickly characterizes the impact of short term PV variability and results in same feeder voltages as the time series simulation of the extreme PV ramps. This provides a fast and accurate method to screen PV interconnections for any potential temporary voltage violations.

3.8.2 Long-Term Variability – Tap Change Analysis

Voltage regulators were designed for slow daily variability of the aggregate feeder load. The high variability and frequent changes in PV output over a long timescale can make the voltage regulation equipment continually change taps, creating additional degradation of the OLTCs [74-76]. Reactive power control of the PV inverters can be used to control the voltage locally [77], but without intelligent coordination, the PV reactive power injections can also create issues with the voltage regulation equipment [78, 79].

The number and the frequency of the PV fluctuations will determine the impact to the number of tap changes. Slow oscillations in PV output will be evened out with the daily load variability, and fast oscillations will occur within the delay window of the regulation equipment. The PV size and variability magnitude also has to be large enough to require a tap or state change in the voltage regulation equipment. If the PV variability matches both these timescale and magnitude requirements, additional tap changes will occur, and the number of which is quantified to study the increased degradation caused by the PV systems.

The impact of solar variability on voltage regulation equipment tap changes is simulated using an agricultural 12kV feeder in California. The feeder peak load is approximately 8.5 MW. The feeder has a substation OLTC, 2 sets of feeder voltage regulators, and six seasonally switching capacitor banks. The feeder topology is shown in Figure 48. The same 1-second irradiance data measured in California mentioned in the previous section is used to model a 3MW PV system using WVM. The PV system is interconnected 5.6 km from the substation, but it is located very close to the feeder regulator. The time delay on the feeder regulator is 45 seconds. The peak load week is selected as the study period.

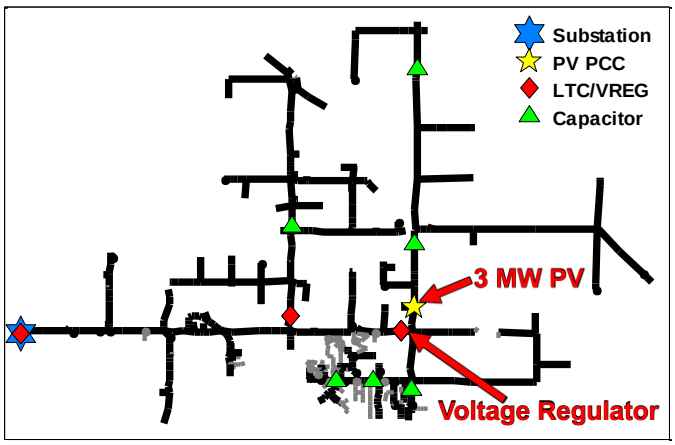


Figure 48. Feeder topology with feeder regulator and PV interconnection locations marked.

Before the interconnection of PV, it should be confirmed that the installation will not have negative consequences on the existing voltage regulation equipment. Sometimes this is simplified to analyzing the maximum power swing from 100% to zero of rated power and limiting the voltage change at the regulator to half the bandwidth, or one tap operation due to full change in output [148]. This over simplifies the analysis because it neglects the changes in load. Studies have shown that if the peak load is fairly correlated with PV production, even with solar variability, tap changes due to solar can actually reduce the overall number of operations over periods of weeks or months [73].

To fully understand all the complexities of the interactions between load and PV through time, quasi-static-time-series (QSTS) simulation tools are needed [84]. Because the solar variability impact on the voltage regulator varies seasonally [73], a long time period such as a year should be simulated at high resolution, which is time consuming and computationally intensive.

An example QSTS simulation is shown in Figure 49 with the results for the number of tap operations over a week. For this system the PV system creates a significant increase of 84% in the number of tap changes. Of course the impact to the number of voltage regulation equipment changes depends on the size of the PV system [80] and the position of the interconnection compared to the regulator [81].

There are many considerations in order to accurately model the number of tap changes on voltage regulation equipment. Both a detailed feeder model and high resolution data are required. It can be difficult to obtain the feeder load data and local high resolution solar irradiance data. The results can vary significantly when using data from another location that does not represent the appropriate local load and solar variability [132]. Local high-resolution irradiance data must be correctly scaled to the expected variability of the specific PV system or range of PV systems. PV systems distributed around the feeder will have significantly less variability than single-point irradiance variability, so distributed PV will have less impact on the voltage regulators [149].

For modeling the distribution system, there are many potential control modes for the voltage regulation devices. Each control mode might not be available in existing software, but the mode must be modeled correctly to analyze the number of tap changes [68]. Voltage regulators commonly used load drop compensation (LDC) to adjust the voltage setpoint according to the current magnitude and power factor. The installed PV system variability impacts the current flow and can interact with the regulator LDC, especially under reverse flow conditions or with smart inverter reactive power control.

Using a detailed model and high resolution data, QSTS simulation provide a method to simulate regulator tap positions and any increase in tap operations. High resolution QSTS does come at a cost. A 1-second resolution QSTS simulation for a 1-year period takes approximately 24 hours of computational time, with the time varying significantly depending on the complexity of the circuit. To improve the interconnection process, a faster method is required for simulating PV variability impacts on the voltage regulation equipment.

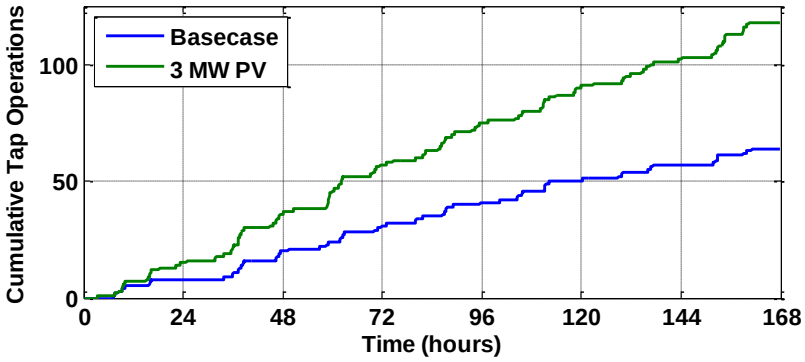


Figure 49. QSTS simulation of week for the number of regulation tap changes for the with and without the 3 MW PV system.

Due to the computational time of high resolution timeseries simulations, a method that does not require QSTS is proposed for faster analysis and interconnection screening of the PV impact on voltage regulation equipment. The tap position of voltage regulation equipment is determined by the primary side voltage and the desired output voltage regulation setpoint. The input voltage is dependent on the downstream load, impedance to the next upstream voltage regulator, and upstream load. Given this, the voltage regulator input voltage can be found for different combinations of load and PV output.

Figure 50 shows the input voltage for the voltage regulator (identified in Figure 48) solved by OpenDSS for various feeder loads and PV power outputs. While Figure 50 was obtained by solving numerous power flows, it could also be numerically calculated with linear sensitivities of the power transfer distribution factors for the primary side voltage and tap position. Figure 50 can be viewed as a lookup table or as a function for the regulator input voltage based on feeder load and PV output. The plotted surface in Figure 50 is the second order polynomial surface fit to the simulated data points signified with blue dots. The function fit accurately represents the simulated data with an R^2 of 0.9999325.

Using the voltage function fit and the annual load and PV profiles, the tap position is determined for every time point in the year along with the total number of tap changes. The load and PV profiles are used to calculate the input voltage for each time

instance. The output voltage can be determined with the tap position of the regulator. Moving through time, if the output voltage is outside the desired range, a tap change is logged. Using the voltage function fit and matrix math avoids having to solve the power flow solution for each time in the year time-series. It is not possible to directly calculate the regulator tap position as a function of PV output and load because the regulator tap position is also based on the previous state and length of the time delays. All time delays, regulator bandwidth, voltage setpoint, and load drop compensation are modeled in MATLAB with the calculated regulator input voltage timeseries as a reference.

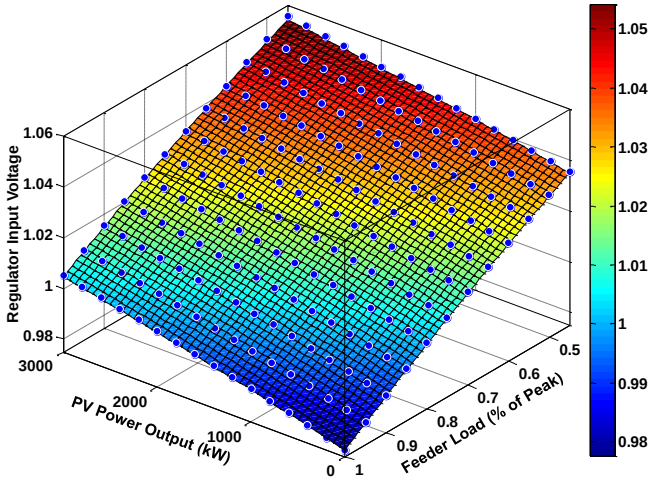


Figure 50. Voltage (pu) at the input of the voltage regulator as a function of PV power output and feeder load. The blue dots represent data points from the power flow solutions, and the surface shows the fit to the simulated data.

The proposed method is compared and validated to the detailed QSTS simulation of the same time period. The analysis of the number of tap changes for a week period using QSTS and the approximation method is shown in Figure 51. While the number of tap changes does not precisely match, the method provides an accurate estimate of the PV impact to the OLTC, but significantly decreases simulation time. The estimated tap change method does not capture all the tap changes due to the solar variability. In this case it was due to the PV system causing slightly different amounts of current flow through the load drop compensation of the voltage regulator in the approximation method. As an approximation, the method is not as detailed as the timeseries simulation,

but it does model the change in tap operations and the general increase or decrease in wear and tear on the regulators.

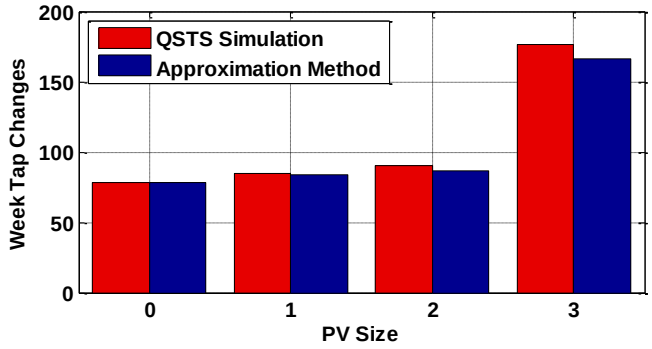


Figure 51. Comparison of the number of tap changes in a week between the QSTS simulation and the proposed method of tap operation estimation.

The estimation method is significantly faster than long time series simulations at high resolution. It does have some initial computational burden of calculating the regulator input voltage dependence on various loads and PV output levels. For this feeder, the method solves approximately 200 power flow solutions and determines the fit in 29.2 seconds. For very short simulations, the proposed estimation method is not efficient because of the computational startup cost. As seen in Figure 52, the approximation method provides significant benefit if the length of the simulation period is longer than a one hour simulation at 1-second resolution. For this feeder performing one year simulations recommended in [73], the QSTS simulation takes around 2 days, and the approximation method takes 1.3 minutes.

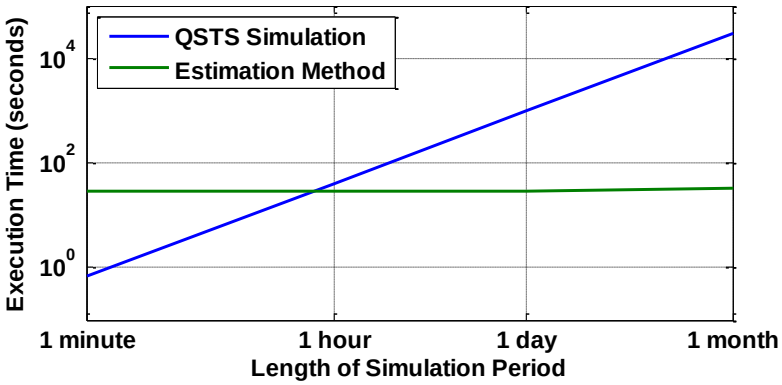


Figure 52. Comparison of the processing time required for the 1-second resolution QSTS simulation to the proposed method of tap operation estimation.

As a means of increasing the efficiency of interconnection studies, two methods are proposed for screening potential PV systems for adverse impacts of PV variability on the distribution system without using time-series simulations. First, a technique to accurately characterize extreme feeder voltages due to high PV ramp rates is demonstrated using voltage regulation equipment locking and expected extreme PV ramping scenarios. Another method is described to determine the potential impact of a PV system on OLTC devices. The methodology is used to model the voltage regulation equipment tap position throughout an entire year and to calculate the number of tap changes. Each of these methods aids in decreasing the complexity and length of time involved in screening potential PV interconnections.

CHAPTER 4: CIRCUIT REDUCTION-BASED METHODS FOR PV INTERCONNECTION SCREENING

4.1 Introduction

With an increasing number of Distributed Generation (DG) being connected on the distribution system, a method for simplifying the complexity of the distribution system to an equivalent representation of the feeder is advantageous for streamlining the interconnection study process. A full detailed model of the distribution system can be time consuming to produce, and a time-series simulation of a large system at a high time-resolution requires significant computational processing [1, 4, 5]. A simplified equivalent circuit will retain the general characteristics of the distribution system and will also reduce the modeling effort required.

This chapter describes an analytical approach that can be used to derive the simplified equivalent representation of the circuit. A distribution feeder, which will typically have hundreds to thousands of line sections and nodes, can be simplified to an equivalent circuit with far fewer line sections and nodes. The reduced circuit maintains the feeder topology and characteristics so that it performs the same in simulation. This representation also preserves any specific buses where voltage or other performance measures are important. These specific buses, or buses-of-interest, represent critical points in the circuit, including: voltage regulation equipment locations, potential PV point of common coupling (PCC) interconnection locations, or extreme voltage locations on the feeder. The buses-of-interest are retained in the reduced circuit maintaining equivalent performance as the full circuit, and all other circuit details are simplified to the minimum amount of necessary information.

One benefit of using a simplified equivalent representation for the feeder is the ability to reduce the feeder complexity to improve the ease of converting the feeder

circuit from one software or analysis package to another. Existing models are often in distribution system programs with limitations for interconnection analysis, such as the available PV models and time-series simulation capabilities of the software. With fewer line segments in the reduced circuit, it would be much simpler and faster to convert feeders from commercial power flow software packages to software like OpenDSS that is open source and can do quasi-static time-series analysis for interconnection studies. The simplified feeder can also provide faster and more accurate interconnection screening criteria by reducing the circuit to a simpler equivalent representation with only the key circuit parameters, which could be used to quickly identify the PV impact risk score for a feeder. Finally, if a full interconnection study is required for a proposed PV system, a simplified equivalent representation would decrease the simulation system size. Time-series analyses of a large distribution system with many feeders, stochastic simulations, or multiple PV study scenarios simulated at a high time-resolution require significant computational processing for full circuit models. Circuit reduction has significant potential benefit for extended high-resolution time-series simulations investigating distribution system regulator controls that take many hours to run [68]. With a reduced circuit model, the simulation could stochastically loop through many different scenarios very quickly. For detailed time-series simulation, this would decrease simulation run times, reduce required processing power, and decrease the computer memory required, while still providing the full accuracy of the full feeder model.

This chapter is organized with the methodology and proofs of equivalence of reduction of a balanced system presented first. Second, the reduction method is implemented for full feeder analysis with thousands of buses. Third, the balanced reduction method is extended to unbalanced systems with unbalanced currents, mixed phase systems, mutual impedance and coupling between phases, line shunt capacitance, and transformer magnetizing current and core losses. Fourth, an algorithm is presented for automatically detecting buses of interest. Finally, the unbalanced reduction is

performed on several real distribution systems in order to demonstrate the robustness of the code under varying feeder topologies.

4.2 Formulating an Equivalent Reduced Representation for Balanced Circuits

Given the limitations of the methods discussed in Chapter 2, a method is developed for reducing the distribution system to an equivalent circuit for performing PV interconnection studies. The reduced circuit must keep the important details like voltage regulators in the circuit while reducing the total number of buses. A method is developed and demonstrated for load bus reduction that combines a load bus into the two adjacently connected buses, thus removing the bus from the circuit. With reduction, all bus voltages and the current going into the network remain the same. In this manner, the circuit is fully equivalent to the original circuit power flow except with fewer buses.

In this section, for simplicity of the derivations, the reduction method assumes balanced loads, balanced wire impedance, no shunt capacitance, and no mutual coupling. The load bus reduction method is also based on the key assumption that all loads on the feeder are fixed current loads. This is an important deviation from many power flow simulations that assume constant power P/Q loads. EPRI has done research on conservation voltage reduction (CVR) that shows every 1% reduction in voltage results in an average of 0.8% reduction in real power, or a CVR=0.8% [150]. From this research, modeling loads as fixed current loads (where CVR=1%), is a valid assumption. This assumption is evaluated in more detail later, and it is shown that the load model selected for simulations also only has a minor impact on the results.

4.2.1 Load Bus Reduction Formulation and Proofs

A novel method is developed and shown to be equivalent in [151] for load bus reduction that combines a load into the two adjacently connected buses, thus removing

the bus from the circuit. The method for load bus reduction is shown for the simplest case with two line sections with impedances Z_1 and Z_2 with loads L_1, L_2, L_3 on each side of the line section shown in Figure 53. The L variables represent the current consumed by the fixed current loads with the units of L being in Amps. If bus 2 is unnecessary in the equivalent circuit, it can be removed by combining L_2 into L_1 and L_3, resulting in a single line section Z_{eq} and only two loads L_{eq1} and L_{eq2}. The resulting reduced circuit has equivalent values for V_1, V_3, and I_s.

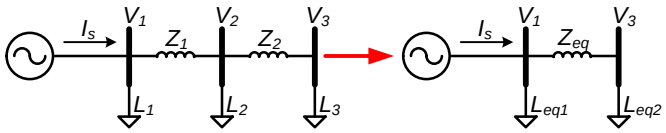


Figure 53. Load bus reduction.

The values for the equivalent circuit are shown in (2) - (4). Note that the impedance between bus 3 and bus 1 remains the same, so all results for short circuit and protection studies are unchanged. The total circuit load is also the same with $L_{eq1} + L_{eq2} = L_1 + L_2 + L_3$.

$$Z_{eq} = Z_1 + Z_2 \tag{2}$$

$$L_{eq1} = L_1 + \frac{Z_2}{Z_1 + Z_2} L_2 \tag{3}$$

$$L_{eq2} = L_3 + \frac{Z_1}{Z_1 + Z_2} L_2 \tag{4}$$

These equations can be derived by equating the voltage drop between V_1 and V_3. The voltage drop must be identical for the full circuit and the equivalent circuit. The voltage drop for the equivalent circuit is

$$V_1 - V_3 = L_{eq2} Z_{eq}. \tag{5}$$

The voltage drop for the full circuit is shown to be the same as the equivalencing method proposed in (2) - (4). The voltage for the full circuit is

$$V_1 - V_3 = (L_2 + L_3)Z_1 + (L_3)Z_2 \tag{6}$$

$$= L_3(Z_1 + Z_2) + L_2 Z_1 \tag{7}$$

$$= L_3(Z_1 + Z_2) + L_2 Z_1 \frac{Z_1 + Z_2}{Z_1 + Z_2} \tag{8}$$

$$= \left(L_3 + \frac{Z_1}{Z_1 + Z_2} L_2 \right)(Z_1 + Z_2) \tag{9}$$

$$= L_{eq2} Z_{eq} \tag{10}$$

By using (2) and (4), the voltage drop is equal on the reduced circuit. In order for the current I_s to be the same entering the circuit, L_{eq1} and L_{eq2} must equal L_1+L_2+L_3, and L_{eq1} can be shown to be the difference between L_1+L_2+L_3 and L_{eq2}, where (15) is equal to the reduction method in (3).

$$L_{eq1} = L_1 + L_2 + L_3 - L_{eq2} \tag{11}$$

$$= L_1 + L_2 + L_3 - \left(L_3 + \frac{Z_1}{Z_1 + Z_2} L_2 \right) \tag{12}$$

$$= L_1 + L_2 - \frac{Z_1}{Z_1 + Z_2} L_2 \tag{13}$$

$$= L_1 + \frac{Z_1 + Z_2}{Z_1 + Z_2} L_2 - \frac{Z_1}{Z_1 + Z_2} L_2 \tag{14}$$

$$= L_1 + \frac{Z_2}{Z_1 + Z_2} L_2 \tag{15}$$

The derivation and formulation of the above equivalent circuit was done to produce equal voltage drop between the equivalent circuit and the full circuit. The equivalent circuit can also be shown to be fully equivalent accounting for line losses. The power consumption by the full circuit including line losses is

$$V_1 L_1 + Z_1 (L_2 + L_3)^2 + V_2 L_2 + Z_2 L_3^{\ 2} + V_3 L_3 \tag{16}$$

The power consumption by the equivalent circuit including line losses is

$$V_1 L_1 + V_1 \frac{Z_2}{Z_1 + Z_2} L_2 + \left(L_3 + \frac{Z_1}{Z_1 + Z_2} L_2 \right)^2 (Z_1 + Z_2) + V_3 \frac{Z_1}{Z_1 + Z_2} L_2 + V_3 L_3 \tag{17}$$

Using the equivalent circuit equation, by expanding the squared term in (17) and in some instances substituting in for $V_1 = V_2 + Z_1(L_2 + L_3)$ and $V_3 = V_2 - Z_2 L_3$, the equation is

$$= V_1 L_1 + \left(V_2 + Z_1\left(L_2 + L_3\right)\right)\frac{Z_2 L_2}{Z_1 + Z_2} + L_3{}^2\left(Z_1 + Z_2\right) + 2Z_1 L_2 L_3 + \frac{Z_1{}^2 L_2{}^2}{Z_1 + Z_2} + \left(V_2 - Z_2 L_3\right)\frac{Z_1 L_2}{Z_1 + Z_2} + V_3 L_3 \tag{18}$$

$$= V_1 L_1 + V_2 L_2\left(\frac{Z_2}{Z_1 + Z_2} + \frac{Z_1}{Z_1 + Z_2}\right) + \frac{Z_1 Z_2 L_2{}^2}{Z_1 + Z_2} + \frac{Z_1 Z_2 L_2 L_3}{Z_1 + Z_2} + L_3{}^2\left(Z_1 + Z_2\right) + 2Z_1 L_2 L_3 + \frac{Z_1{}^2 L_2{}^2}{Z_1 + Z_2} - \frac{Z_1 Z_2 L_2 L_3}{Z_1 + Z_2} + V_3 L_3 \tag{19}$$

$$= V_1 L_1 + V_2 L_2 + Z_1 L_2{}^2\left(\frac{Z_2}{Z_1 + Z_2} + \frac{Z_1}{Z_1 + Z_2}\right) + L_3{}^2\left(Z_1 + Z_2\right) + 2Z_1 L_2 L_3 + V_3 L_3 \tag{20}$$

$$= V_1 L_1 + V_2 L_2 + \left(Z_1 L_2{}^2 + 2Z_1 L_2 L_3 + Z_1 L_3{}^2\right) + Z_2 L_3{}^2 + V_3 L_3 \tag{21}$$

$$= V_1 L_1 + Z_1\left(L_2 + L_3\right)^2 + V_2 L_2 + Z_2 L_3{}^2 + V_3 L_3 \tag{22}$$

Thus, the total power for the equivalent circuit, shown in (22), is the same as the total power for the full circuit shown in (16). Note that while the line losses are accounted for in the equivalent model and the total power of the circuit is equal, if the line losses are directly calculated for each model, the I^2R losses will be different for the current flow. By moving part of L_2 to the first bus, the line losses are included in the movement of the fixed current load to the higher voltage. The line losses will always be correct, as shown above, but the line losses associated with L_2 in the reduced circuit is the combination of additional current flow along Z_{eq} and the increased power consumption from placing part of the fixed current load at a slightly higher voltage V_1.

The above process for reducing a single load bus can be repeated any number of times (recursively) to combine each load current into the load currents on either side of it using equations (2) - (4). Any chain of loads can be reduced into two buses. For example, the seven load buses shown in Figure 54 can be combined into two buses (V_1 and V_7). Each fixed current load in between the buses-of-interest is combined with the load currents on either side in proportion to the line impedances.

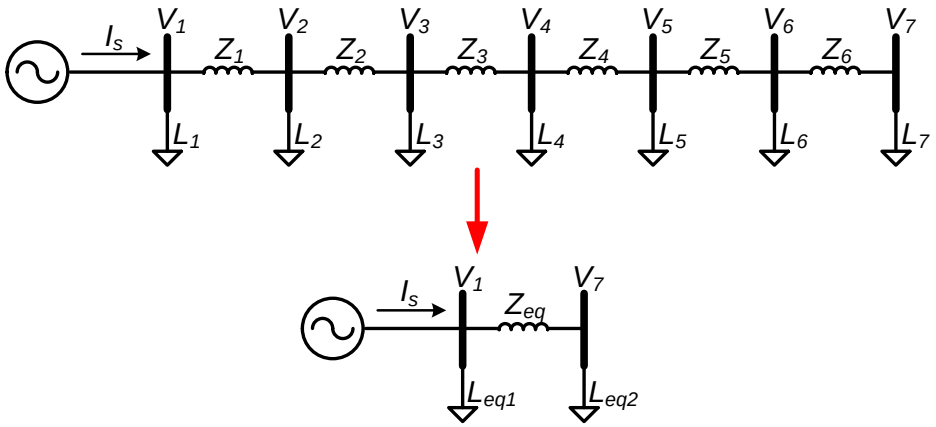


Figure 54. Multiple load bus reduction.

Note that if the loads are equally spaced along the line where all line impedances between the buses are equal, (3) and (4) show that the reduced load bus is equally split between each adjacent bus. When the loads are equal in magnitude in addition to equally spaced, the equivalent circuit is half the load current at either end of the line section.

For any number of loads or feeder length, reducing a long section such as shown in Figure 54 will result in half of the load current at the beginning of the line section and half of the load current at the end. The reduction of uniform loads to two equal loads at either end is also shown in [110]. If the circuit in Figure 54 has uniform loads with magnitude L and impedance Z between all of them, the equivalent circuit is

$$Z_{eq} = 6 \times Z \tag{23}$$

$$L_{eq1} = \frac{7}{2} L \tag{24}$$

$$L_{eq2} = \frac{7}{2} L \tag{25}$$

The method of load bus reduction allows any string of load buses to be combined, but realistic distribution feeders contain many branching sections and laterals. If the voltage on the branch or lateral is not required in the reduced circuit, all loads on the branch can be reduced by combining the loads onto the location of the branch split from the path that contains buses-of-interest. This is shown in Figure 55 where the equivalent

load current at bus 1 is the sum of the load currents on the lateral. The method can be performed when the voltage V_4 and the voltage drop between V_1 and V_4 are not desired in the equivalent circuit.

The reduced circuit will have the same measured voltages at the buses-of-interest (1, 2, and 3) and the same current flowing into the network. The reduced circuit is fully equivalent and accounts for the line losses in Z_3 because the loads are fixed current loads. For example, the L_4 load current when moved to bus 1 is connected at a slightly higher voltage bus in the distribution system. The difference in voltage between bus 1 and bus 4 is due to the line loss from the current flowing to L_4, so placing the fixed current load at the higher voltage equals the total power consumption of the original circuit for the load and the line loss. The power flowing into the lateral shows the equality of moving L_4 to V_1. In this simple case the current flowing into the lateral I_L=L_4. The total power in the lateral is

$$P = L_4 * V_4 + (L_4)^2 Z_3 . \tag{26}$$

With some manipulation, the total power in the lateral (26) is shown to equal the total power when L_4 is moved to bus 1 at V_1.

$$L_4 * V_4 + (L_4)^2 Z_3 = L_4 (V_4 + L_4 Z_3) = L_4 V_1 . \tag{27}$$

While the total power is the same and the line losses are always fully accounted for the equivalent circuit, the line losses directly calculated using the I^2R losses will be different. This is similar to the previous discussion for load bus reduction where by moving L_4, the line losses are included in the movement of the current source to the higher voltage. Line losses will always be correctly modeled in the equivalent, as shown in (26) and (27), but the circuit line losses can no longer be calculated using I^2R.

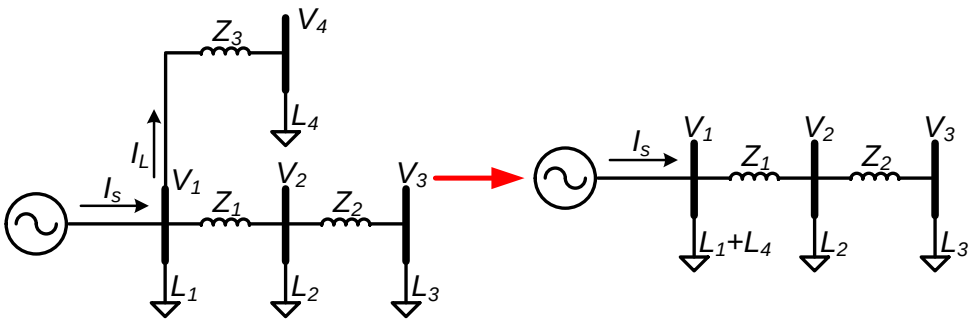


Figure 55. Branches or laterals combination.

Any buses after a bus-of-interest can be reduced similarly to branch or lateral combination. If the voltage at the end of the lateral is not required, any bus downstream of a bus-of-interest is handled like a branch and can be combined back to the branch of interest, as shown in Figure 56. Note that the voltage at V_2 is the same in both circuits because

$$V_2 = V_1 - Z_1\left(L_2 + L_3 + L_4\right). \tag{28}$$

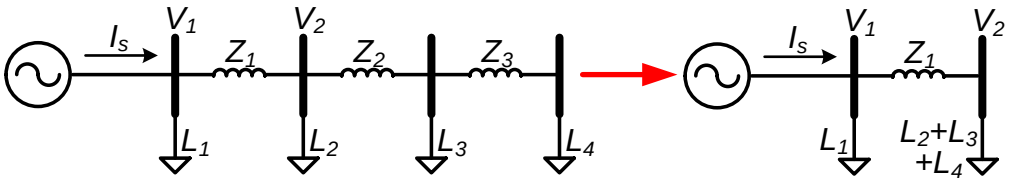


Figure 56. Downstream loads combined into a bus-of-interest.

If there is a bus-of-interest on a branch in the feeder, the branch cannot be removed in the reduced circuit; otherwise the topology of the feeder would be modified in the equivalent circuit. The bus where the network splits must also remain if there is a bus-of-interest on each branch, but all loads on the branches can be reduced. For example, if V_3 and V_5 in Figure 57 are buses-of-interest, the circuit can be reduced to three buses and three load currents, where the three equivalent load currents are the sum of the load currents in between each bus-of-interest.

$$L_{eq1} = L_1 + \frac{Z_2}{Z_1 + Z_2} L_2 + \frac{Z_4}{Z_3 + Z_4} L_4 \tag{29}$$

$$L_{eq2} = L_3 + \frac{Z_1}{Z_1 + Z_2} L_2 \tag{30}$$

$$L_{eq3} = L_5 + \frac{Z_3}{Z_3 + Z_4} L_4 \tag{31}$$

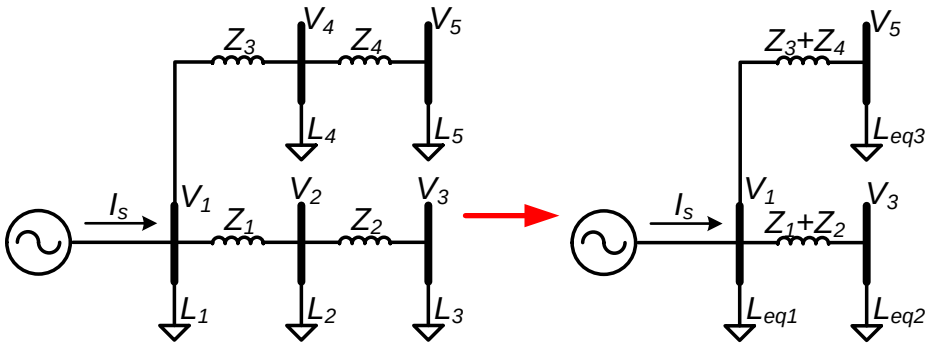


Figure 57. Two buses-of-interest creating a branching equivalent circuit.

4.2.2 Discussion of the Fixed Current Load Assumption

The proposed circuit reduction method is based on the key assumption that all loads on the feeder are fixed current loads, and not fixed P/Q loads as is commonly the assumption for power systems analysis and power flow simulations. This section discusses the differences between the load model types used for simulations and any deviations that may be introduced by modeling loads as fixed current loads instead of fixed P/Q loads.

The load type determines the model for the power consumption as a function of the voltage. As part of their Distribution Green Circuits program, EPRI has done experimental research on distribution feeders using conservation voltage reduction (CVR), showing empirically that every 1% reduction in voltage results in an average of 0.8% reduction in real power, or a CVR=0.8% [150]. For a fixed current load model, the power consumption is directly related to the voltage; therefore, CVR=1% for fixed current loads. Conversely, the power consumption does not change for fixed P/Q loads, which corresponds to a CVR=0%. Loads are also sometimes modeled as fixed

impedance loads where the power is a function of the square of the voltage, in which case CVR=1.99%. From the point of view of power consumption as a function of voltage, modeling loads as fixed current loads is a valid assumption (CVR=1% vs. CVR=0.8% from EPRI's Distribution Green Circuits research), and may even be more accurate than modeling loads as fixed P/Q or fixed impedance.

While the power consumption as a function of voltage depends on the load model, there is very little difference in simulation results between different load model types. During the circuit model creation, the load types are selected for the feeder, and the load allocation process tunes the simulation model results to match the measured data from the feeder. If the load measurements are taken at the substation, when the load is allocated around the feeder, the simulation results must verify that the power at the substation is still the same as measured. In this case, for a fixed current load model, no tuning will be required because the substation voltage times the sum of all the load currents will always equal the measured power at the substation. If fixed P/Q load models are used, an iterative process must be used to match the sum of power consumption of the loads and all line losses to the measured power at the substation. In the event that the feeder data provided contains load measurements at the loads instead of the substation, the two load models switch roles in their need for calibration, causing the fixed current model to require tuning while the fixed P/Q model will not. For more information on load allocation see Section 2.4.1 in [110]. The load allocation process was performed for the full detail distribution feeder shown in Figure 58 using the load measurements at the substation. The models were calibrated to match the measured real and reactive power for each phase with a total feeder load of approximately 6 MW at 0.9 power factor. Simulations were run for three load model types: fixed P/Q, fixed current, and CVR type. The "CVR load" represents the results from [150] with CVR=0.8% for real power and CVR=3% for reactive power. The per unit phase voltages for each load type are shown in Table 5.

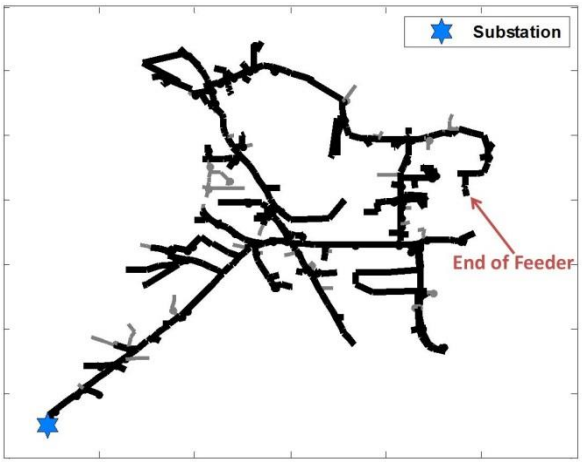


Figure 58. Example feeder for load allocation of different load types.

Table 5. End of feeder voltages (pu) for the feeder model in Figure 58 with different load types.

	Power	Current	CVR
Phase A Voltage (pu)	1.01823	1.01835	1.01843
Phase B Voltage (pu)	1.02162	1.02153	1.02150
Phase C Voltage (pu)	1.02354	1.02331	1.02320

Table 6 demonstrates that the simulation results for a feeder are very similar independent of the type of load model. Table 6 also shows that using a fixed current load model is much closer to the actual feeder response, as measured by EPRI's CVR research.

Table 6. Average percent difference for end of feeder voltages with different load type models.

Current Vs. Power	Current Vs. CVR	Power Vs. CVR
0.015%	0.007%	0.022%

The results for the real distribution feeder model above are very small, but the theoretical maximum error will be shown using an extreme case and the simple circuit in Figure 59. The same three load models are investigated, and the circuits are calibrated to have the same power flow at V_1 of 1000+ j200 kVA. These extreme cases will use the full allowed voltage range 1.0±0.05 pu, with the ΔV between V_1 and V_2 equal to 0.05 pu for the base case simulation. As seen in Table 7, for this simple circuit, the load

allocation and calibration process makes the simulation voltages equal for the different load types. For any new study scenario that would change the voltages, the percent change in the load power consumption due to the new voltage depends on the load model type. For example, simulations with new PV, different voltage control algorithms, the addition of capacitors, and expansion of existing loads will all present differences in simulation results between fixed current and fixed P/Q loads. In this case, the generator at V_1 has changed the voltage setpoint from 1.0 pu to 1.05 pu and the simulation results in Table 7 deviate between load models. Even for this extreme case, the fixed current load model is within ~0.0025 pu voltage of the fixed P/Q load model. As shown in Table 8, the fixed current load model is much more accurate compared to the CVR voltage than fixed power loads.

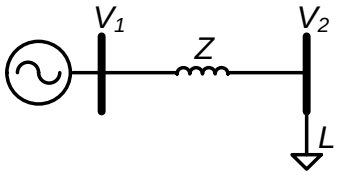


Figure 59. Simple circuit for discussion about load model types.

Table 7. Bus voltages for two scenarios with different load type models for the circuit in Figure 59.

		Power	Current	CVR
Base Case V_1 setpoint=1.0	V_1 (pu)	1.0	1.0	1.0
	V_2 (pu)	0.95	0.95	0.95
Increased V_1 setpoint=1.05	V_1 (pu)	1.05	1.05	1.05
	V_2 (pu)	1.0027	1	0.99974

Table 8. Percent difference in simulation voltages for different load type models.

Current Vs. Power	Current Vs. CVR	Power Vs. CVR
0.267%	-0.033%	0.300%

The load model type does not significantly impact simulation results. For a full feeder model, the simulation differences were less than 0.025% for different load models. Using an extreme case, the maximum possible error between fixed power and fixed

current load models is less than 0.3%. Compared to empirical CVR research in [150], a fixed current load model is more accurate representation of real feeders than a fixed P/Q load and would have less model error compared to average distribution system loads. Therefore, the assumption of fixed current loads does not negatively impact the circuit reduction results.

4.2.3 Example of Balanced Reduction

The formulation and equivalence of the circuit reduction method is applied to an example distribution feeder in Figure 60 to demonstrate the reduction steps. Each step of the reduction process is explained in detail, and the equivalent circuits with all circuit parameters for each step are shown. The equivalence is validated during each step by simulating the shown circuits in PowerWorld Simulator to solve the power flow for voltages and currents. In the figures, voltages are line to line, current is per phase, and impedances are in ohms. The loads are balanced 3-phase, fixed-current loads. The loads are labeled in the figures with their rated power in kVA at the 19.8 kV rated voltage, but as fixed current loads their actual power consumption varies with voltage at the bus. The current of each load is constant and can be calculated by dividing the rated kVA by the rated voltage.

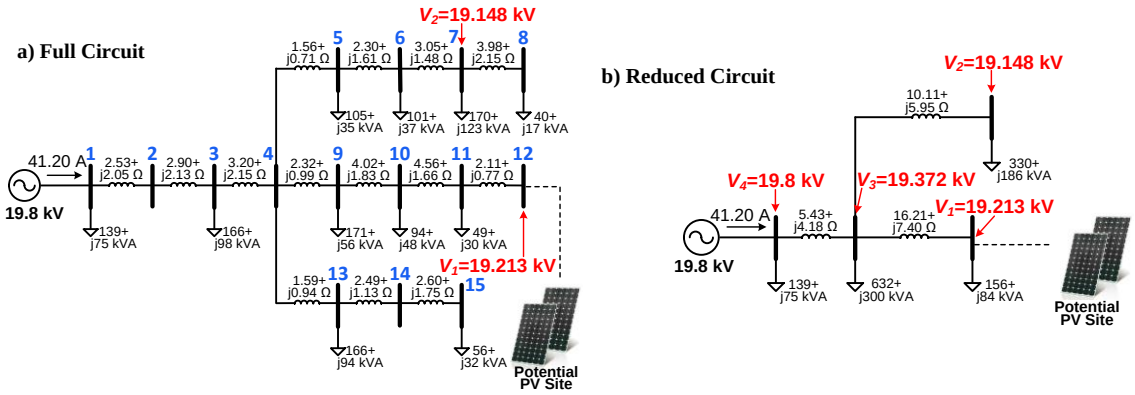


Figure 60. Full feeder reduction. a) original 15-bus feeder, b) final, simplified circuit.

Reduction Steps:

Step 1: User selects any specific buses that should remain in the reduced circuit, in this case, V_1 and V_2 are selected. The algorithm automatically identifies additional buses of interest such as capacitors, voltage regulators, step transformers between buses of interest, and junctions required to maintain the topology in the reduced circuit. This step would identify buses 1 and 4 in Figure 60 as additional buses of interest.

Step 2: Remove all buses without objects on them or junctions of multiple lines. This removes all lines that are at the end of a feeder without a load connected to them. It also removes all unnecessary buses that were originally only used for line routing in visualizations and calculating line lengths. This step removes buses 2 and 14 in Figure 60.

Step 3: Reduce all loads not on the paths to buses of interest. All loads are condensed to the nearest upstream bus on a path between the substation and a bus of interest. This often moves loads from their interconnection on the end of a triplex line to the medium voltage feeder backbone. This step reduces buses 8, 13, and 15 in Figure 60.

Step 4: Perform load bus reduction using (2)-(4) to recursively move loads to the adjacent buses. This step removes buses 3, 5, 6, 9, 10, and 11 in Figure 60.

After performing circuit reduction, the 15-bus feeder is reduced to 4 buses. During the process, two additional buses-of-interest were added at the generator and at the junction between the two buses-of-interest to maintain the feeder topology. As seen in Figure 60, the solved power flow in PowerWorld results in the same voltages and currents as the full feeder model during each step of the reduction process. The steps and resulting calculated parameters are shown for the process to demonstrate the method, and simulations validate the equivalence of the reduced feeder model.

The purpose of the circuit reduction method is to study the impact of variable renewable generation on the distribution system, so validation is performed by simulating

the interconnection of PV on the system. Figure 61 contains the full circuit model along with the reduced circuit and the two potential PV interconnection study locations at V_1 or V_2.

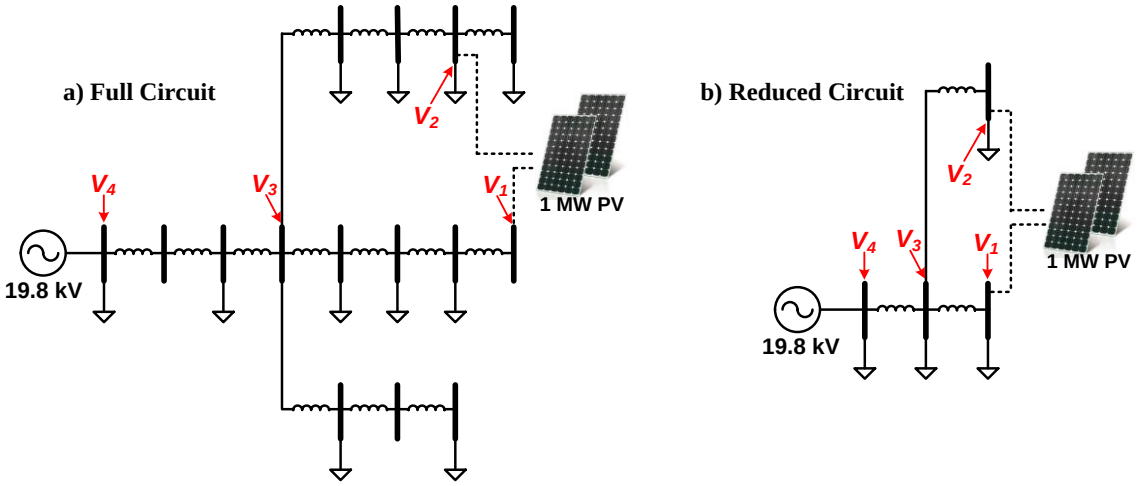


Figure 61. a) Full feeder circuit and b) reduced circuit with potential PV interconnection study locations at V1 or V2.

Studying the impact of distributed generation, specifically PV, is done using both static snapshot analyses and time-series simulations. For the static steady-state analysis validation, the results are shown in Table 9 for a 1 MW PV plant connected at either V_1 or V_2 compared to the base case without solar. Note that the feeder topology is maintained and the voltages at the buses-of-interest are exactly equal for the reduced circuit for all three PV scenarios.

Table 9. Voltages at buses-of-interest for the full feeder circuit and the equivalent reduced circuit for different PV connection scenarios.

	No Solar		1 MW PV at V_1		1 MW PV at V_2	
	Full	Reduced	Full	Reduced	Full	Reduced
Bus V_1	19.213 kV	19.213 kV	20.275 kV	20.275 kV	19.483 kV	19.483 kV
Bus V_2	19.148 kV	19.148 kV	19.412 kV	19.412 kV	19.923 kV	19.923 kV
Bus V_3	19.372 kV	19.372 kV	19.637 kV	19.637 kV	19.643 kV	19.643 kV
Bus V_4	19.800 kV	19.800 kV	19.800 kV	19.800 kV	19.800 kV	19.800 kV

The same three simulations of the base case without solar, 1 MW PV at V_1, and 1 MW PV at V_2 are performed as time-series simulations for a 1-day period at 15 minute resolution. For the simulations, the load varies according to a standard load profile with the peak load in late afternoon. The peak load is shown in Figure 60, and all loads are varied together by a multiplier the rest of the day to match the feeder load profile. The impact on the voltages at the four buses-of-interest due to variations in the load is shown in Figure 62a. As seen in Figure 62a, the reduced circuit has the same results as the full circuit even as the loads change throughout the day. The one-day simulations for a 1 MW PV plant connected at either V_1 or V_2 are shown in Figure 62b and Figure 62c respectively. The solar output profile for a cloudy day is simulated to show the impact of solar variability on the voltage and the corresponding time-series accuracy of the reduced model.

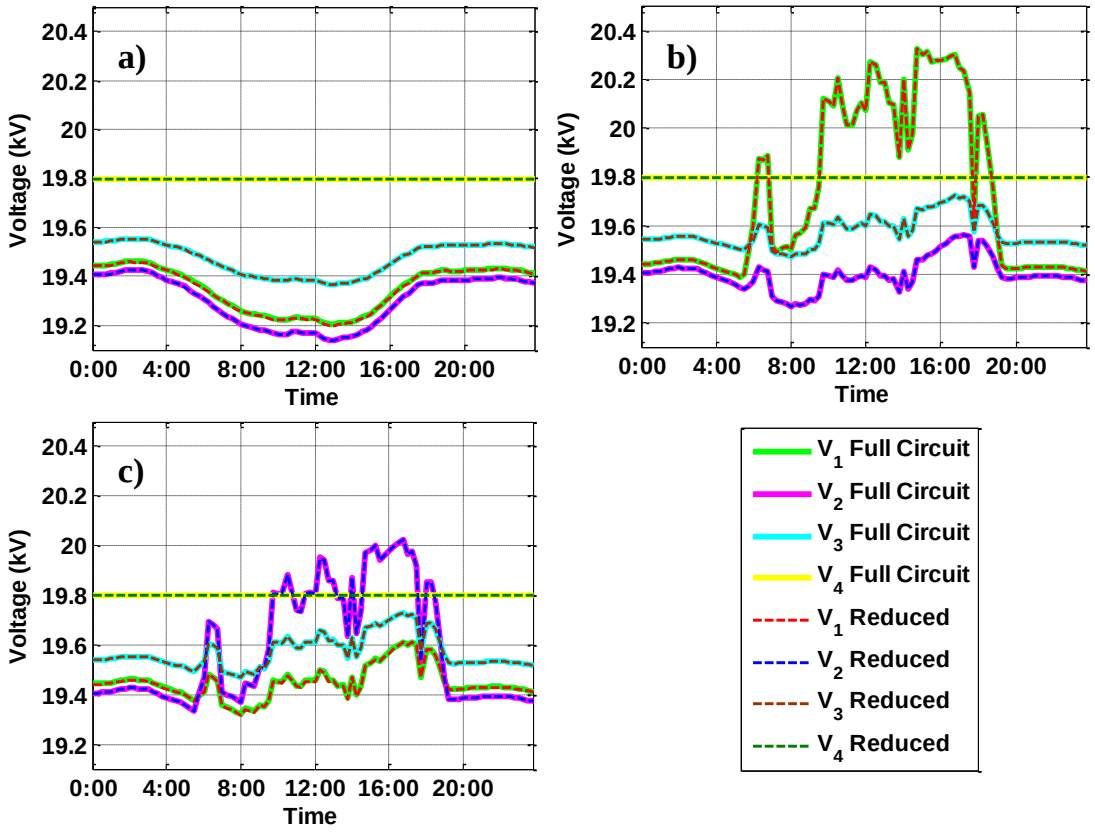


Figure 62. Simulation of the full circuit and reduced circuit for a) base case without solar, b) 1 MW PV at V1, and c) 1 MW PV at V2.

The reduced circuit is shown to be equal to the full feeder model for both snapshot simulations and time-series simulations with solar interconnected at two locations. The reduced circuit can accurately represent the time-varying nature of PV on the grid.

4.3 Implementing Circuit Reduction for Large Systems

The same reduction methodology can be applied to a very large complicated distribution system with distributed PV, as shown in Figure 63. To apply the method to a large circuit with hundreds or thousands of components, the load bus reduction was implemented in MATLAB for full automation. The distribution system modeling is done using OpenDSS, which is an open source 3-phase distribution system simulator from EPRI [117]. MATLAB communicates with OpenDSS through the COM interface to obtain the circuit parameters such as line impedances, line lengths, and load ratings. The circuit reduction is performed in MATLAB and the resulting reduced circuit is then saved back out to OpenDSS where the power flow simulations are performed for validation.

In the previous section, circuit reduction was performed on a single large PV interconnection. The same circuit reduction process can be used for distributed rooftop PV. If there are a large number of PV interconnections, they can be reduced as equivalent PV plants with the same voltages at buses of interest. For example, the feeder in Figure 63 has 70 PV interconnections that are reduced to three equivalent PV plants with all buses of interest being equivalent in the reduced circuit. The user selected buses of interest for this analysis are bus 10 and bus 13, which is selected due to the high voltage seen in simulation with PV. All other buses in the reduced equivalent circuit are automatically identified as additional buses of interest by the algorithm. Each capacitor bank (buses 5, 6, and 7) must remain in the reduced circuit as a bus of interest to model the reactive power output as well as any capacitor switching. Buses 3 and 4 are identified as necessary to maintain the topology of the reduced circuit. Finally, the transformers

between buses of interest (buses 1, 2, 8, 9, 11, and 12) must also remain in the final circuit. The process for reducing PV plants is the same as reducing loads for Steps 3 and 4 of the reduction. The voltage profile for the full feeder model can be seen in Figure 64 along with the reduced circuit that has equivalent voltages at the buses of interest.

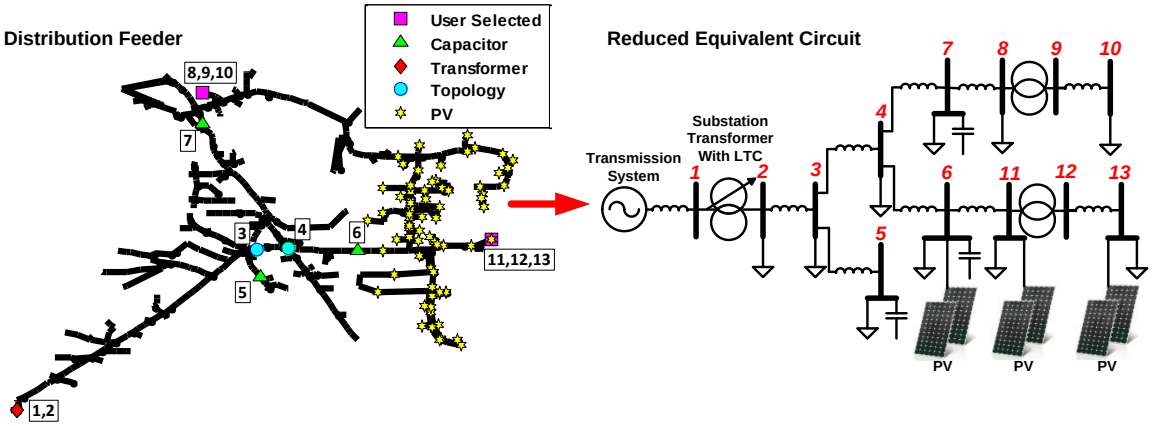


Figure 63. A full distribution system feeder with 70 distributed rooftop PV systems reduced to a simple equivalent representation.

The extremely complex system can be reduced to a simple circuit with only a few parameters that wholly and accurately represents the currents and voltages at all buses of interest in the equivalent circuit. The voltage profile for the full feeder model can be seen in Figure 64 with equivalent voltages at the buses of interest in the reduced circuit. The reduced circuit also maintains all distances, short circuit currents, and impedances between buses of interest. During the reduction, all other complexity and bus voltages in the original circuit are lost. This is advantageous if the distribution engineer is not interested in the voltage at those thousands of other buses. If the information or characteristics of a bus are desired, it can simply be selected as a bus of interest before reduction.

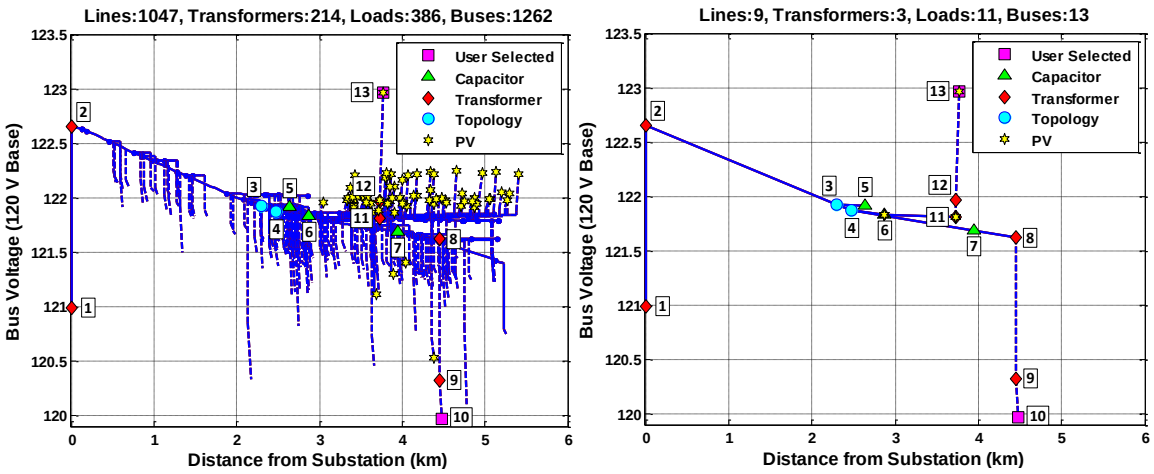


Figure 64. Voltage profile with distributed rooftop PV for A) the full distribution feeder, and B) the reduced equivalent circuit.

The equivalence of the reduced circuit is analyzed by comparing the voltages for the snapshot simulation shown in the voltage profile plots. The differences for the power flow solution voltages are in the order of 10^{-6}. This error is likely due to small rounding differences in the process, and the differences are small enough to be insignificant during the interconnection process.

Table 10. Voltages for Buses of Interest with PV

Bus	Full (kV)	Reduced (kV)	Difference (pu)	Diff (120V base)
1	115.9471	115.9471	-3.46E-08	-4.15E-06
2	20.2375	20.2375	-8.16E-07	-9.79E-05
3	20.1170	20.1170	7.52E-07	9.02E-05
4	20.1088	20.1088	7.49E-07	8.99E-05
5	20.1156	20.1156	7.52E-07	9.03E-05
6	20.1028	20.1028	8.96E-07	1.07E-04
7	20.0787	20.0787	3.68E-07	4.42E-05
8	20.0684	20.0684	-2.22E-06	-2.66E-04
9	0.4813	0.4813	4.28E-07	5.14E-05
10	0.4799	0.4799	4.28E-07	5.14E-05
11	20.0993	20.0993	-1.93E-06	-2.31E-04
12	0.4878	0.4878	-1.92E-06	-2.31E-04
13	0.4919	0.4919	-1.90E-06	-2.28E-04

A time-series analysis was conducted as well to show the preservation of accuracy with varying load, voltage regulation equipment, variable PV output, and switching

capacitors. For the simulation in Figure 65, the voltages are shown at the selected buses of interest for the full model and the reduced circuit.

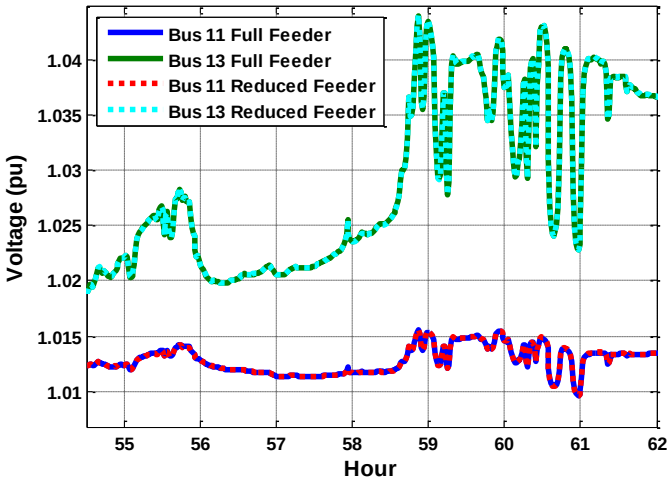


Figure 65. Time-series analysis with distributed rooftop PV, comparison of full vs. reduced circuit for selected buses of interest.

Circuit reduction has significant advantages in that it takes less memory and less processing time for simulations. Table 11 shows the improvements in reducing the circuit. One of the most significant benefits of circuit reduction is the decreased simulation time for long high-resolution time-series simulations. For example, a one-week simulation at 1-second resolution that takes 14 minutes to run for the full distribution model performs with the same accuracy in 15 seconds for the reduced circuit.

The magnitude of the reduction and the number of buses in the reduced circuit depends on how many buses of interest are selected (*n*), plus some buses of interest to represent the topology of the distribution system. The final reduced circuit will contain between n and 2**n*, with no more than twice the selected buses of interest in the reduced circuit. For example, a distribution feeder with 6 capacitor banks and 4 voltage regulators would reduce to less than 20 buses, independent of the number of loads or the length of the feeder. The buses of interest are retained in the reduced circuit, maintaining

equivalent performance as the full circuit, and all other circuit details are simplified to the minimum amount of necessary information.

Table 11. Magnitude of Reduction from Full Circuit

	Full Circuit	Reduced Circuit	% of Original
Time (seconds) to perform a week simulation at 1-second resolution	837.94	15.48	1.85%
Circuit – Number of Lines	1047	9	0.86%
Circuit – Number of Transformers	214	3	1.40%
Circuit – Number of Loads	386	10	2.59%
Circuit – Number of Buses	1262	13	1.03%

A balanced circuit reduction methodology was presented for simplifying entire feeders with thousands of buses to only specified buses of interest while maintaining accuracy and the feeder topology. The method is demonstrated with distributed rooftop PV on a 1262-bus feeder with two buses of interest that is reduced to a 13-bus circuit. The accuracy of the method was shown for both a snapshot as well as a time-series analysis with the error generally in the order of 10^{-6}.

4.4 Formulating an Equivalent Reduced Representation for Unbalanced Circuits

The balanced circuit reduction method [151, 152] presented in the previous sections is expanded to remove the main assumptions and simplifications about a balanced distribution system. The unbalanced circuit reduction method includes mixed-phase distribution systems, unbalanced currents, coupling between power lines, mutual impedance, single-phase loads, and single-phase lines. This is an important advancement from the balanced circuit reduction because most distribution systems in the United States have significant amounts of unbalance caused by single-phase loads and laterals. Although the circuit complexity is increased significantly, it is important that the reduction method can be implemented on a realistic distribution system.

The unbalanced circuit reduction algorithm presented will also account for shunt impedances that were previously ignored or assumed to be zero. This includes the line charging shunt capacitance and non-ideal transformers with core losses. With the zero line charging assumption in the balanced reduction, lines were easily removed during the reduction without impacting the accuracy. Transformer magnetizing current introduces a shunt resistance and shunt reactance that creates no-load losses on the transformer that cannot be directly included into the series impedances of lines. Both of these shunt impedances are captured in the unbalanced circuit reduction where the reduced circuit will be equivalent to the full model.

The assumption that the loads are modeled as fixed current loads remains in the unbalanced reduction. As shown in Section 4.2.2, this assumption may be more accurate than a constant power P/Q load model, and the load model makes little different in the results.

The circuit reduction algorithm uses sequence components to handle the mutual impedances and unbalanced loads. Sequence components require that the impedance matrix is symmetrical with the mutual terms all being equal. This is not necessarily the case unless the lines are perfectly transposed at equal distances. Sequence components are regularly used for distribution system modeling, especially for underground cabling, as an approximation and simplification of the actual system.

New algorithms have been developed for each step in order to handle unbalanced circuits and shunt impedances, but the main reduction steps follow the same process as the balanced circuit reduction.

Reduction Steps:

Step 1: The user selects any specific buses that should remain in the reduced circuit. The algorithm automatically identifies additional buses of interest such as capacitors, voltage regulators, step transformers between buses of interest, and junctions required to

maintain the topology in the reduced circuit. For unbalanced circuits, the location of any change in number of phases between buses of interest must be added as a topology bus of interest.

Step 2: Remove all buses without objects on them or junctions of multiple lines. It removes all unnecessary buses that were originally only used for line routing in visualizations and calculating line lengths.

Step 3: All laterals and loads not on the paths to buses of interest are reduced up into the path between buses of interest. This often moves loads from their interconnection on the end of a secondary triplex line to the medium-voltage feeder backbone.

Step 4: Perform load bus reduction to recursively move loads into the adjacent buses.

Each of the new algorithms for unbalanced circuit reduction are described in the following sections.

4.4.1 Sequence-Component Kron Reduction with Shunt Capacitance

The second step in the reduction process removes buses that do not have any circuit objects on them. These buses are solely for georeferencing to allow the cables to be plotted in a map fashion, and the cable lengths can be derived from the georeferenced points. For the balanced circuit reduction, the series impedance of each line connected to the bus was simply added together, and the bus was removed. In order to include the mutual impedances between lines and the line charging capacitance, a sequence-component Kron reduction method is presented to perform the reduction step shown in Figure 66.

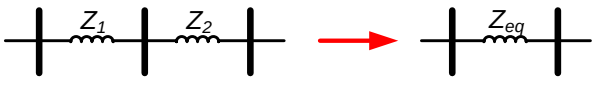


Figure 66. Removing buses without circuit objects.

To begin the reduction, the positive and zero sequence Y_{bus} admittance matrix is formed for the lines connected to the bus. The negative-sequence impedance is assumed to equal the positive sequence. The line shunt capacitance terms are added to the Y_{bus} matrix on the diagonal terms using the pi-model. The Y_{bus} matrix is as follows:

$$Y_{bus} = \begin{bmatrix} \frac{1}{Z_1} + \frac{j\omega C_1}{2} & -\frac{1}{Z_1} & 0 \\ -\frac{1}{Z_2} & \frac{1}{Z_1} + \frac{1}{Z_2} + \frac{j\omega C_1}{2} + \frac{j\omega C_2}{2} & -\frac{1}{Z_2} \\ 0 & -\frac{1}{Z_2} & \frac{1}{Z_2} + \frac{j\omega C_2}{2} \end{bmatrix} \tag{32}$$

where C_1 represents the shunt line charging capacitance for line 1. The Y_{bus} matrix is formed separately for each the positive and zero sequence impedances using the positive and zero sequence line impedances and shunt capacitance respectively. To remove the middle bus, Kron reduction is applied using the below formulas.

$$\begin{aligned} Y_{11}^{new} &= Y_{11} - \frac{Y_{12}Y_{21}}{Y_{22}} \\ Y_{12}^{new} &= Y_{13} - \frac{Y_{12}Y_{23}}{Y_{22}} \\ Y_{21}^{new} &= Y_{31} - \frac{Y_{32}Y_{21}}{Y_{22}} \\ Y_{22}^{new} &= Y_{33} - \frac{Y_{32}Y_{23}}{Y_{22}} \end{aligned} \tag{33}$$

Kron reduction is applied to both the positive and zero sequence Y_{bus} matrices. After Kron reduction, the new equivalent line impedances are the Y_{21}^{new} and Y_{12}^{new} terms, which are equal in the symmetrical matrix. The sum of the new Y_{bus} matrix represents the total line charging capacitance on the equivalent line. The pi-model is used as an approximation with equal shunt capacitance on either end of the line.

Sequence-component Kron reduction is applied to each bus without a circuit object. The algorithm loops through each of the buses, forms the positive and zero

sequence Y_{bus} matrix around that bus, performs Kron reduction, creates the new line, and disables the old lines connected to the bus being reduced. This reduction does not work if the two lines connected to the bus have different number of phases. For this case, the bus remains in the circuit as a topology bus of interest.

Note that with the assumptions of balanced currents, no shunt capacitance, and no mutual impedance, the sequence-component Kron reduction method is the same as the balanced circuit reduction. Buses without loads are able to be reduced using sequence-component Kron reduction without having to assume a balanced system.

4.4.2 Sequence-Component Norton Equivalent

The third step in the reduction process is to combine all branches and laterals not directly in the current stream between the substation and a bus-of-interest. If the voltage on the branch or lateral is not required in the reduced circuit, all loads on the branch can be reduced by combining the loads onto the location of the branch split from the path that contains buses-of-interest. All loads are condensed to the nearest upstream bus on a path between the substation and a bus of interest. This often moves loads from their interconnection on the end of a triplex line to the medium voltage feeder backbone.

The balanced circuit reduction method simply moved the sum of all loads on the lateral to the bus along the path to a bus of interest. When the shunt impedances are included in the circuit, moving the fixed current loads is not equivalent. For example, with a non-ideal transformer, the transformer core losses prevent the load from being moved to the primary system and the transformer from being removed. To include line charging and transformer magnetizing current, a sequence-component Norton equivalent is developed to remove any laterals or sections of the circuit not along the paths to buses of interest.

Using the assumption that loads are fixed-current, the circuit looks very similar to fundamental circuit analysis problems. For example, calculating the Norton equivalent in

Figure 67 is straight-forward. The transformer winding losses are shown as Z_S, core losses as R_C, and magnetizing reactance as X_M. The Norton equivalent impedance Z_{EQ} is the look-in impedance for the circuit with the current sources open. The Norton equivalent current source is the current that would flow into the circuit with the head of the lateral shorted to ground.

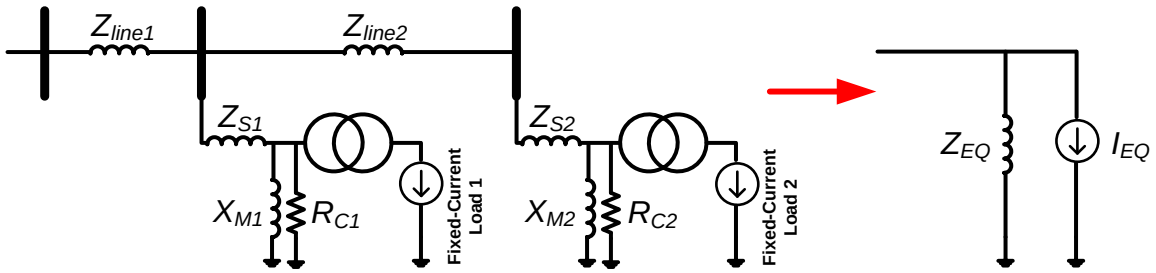


Figure 67. A lateral with two transformers and loads reduced to a Norton equivalent.

For unbalanced three-phase circuits, the Norton equivalent must be done using sequence components. The positive and zero sequence look-in impedances for Z_{EQ} are found with the open-circuit loads, and the sequence currents are calculated for the head of the lateral shorted to ground. Using the sequence-component Norton equivalent allows all sections of the circuit not along buses of interest to be reduced, even with line shunt capacitance, transformer magnetizing current, and unbalanced loads.

The sequence-component Norton equivalent is implemented in OpenDSS to loop through all laterals and calculate the equivalent values. The equivalent impedance is calculated by turning off all downstream loads in the section of the circuit and measuring the voltage and current. The sequence voltage divided by the sequence current will provide the look-in sequence impedance for the Norton equivalent. The Norton equivalent current is calculated by measuring the sequence current flowing into the circuit with the loads connected and subtracting the current that would flow into the equivalent impedance found in the previous step. The new sequence-component shunt

reactor and fixed current load are added to the circuit in OpenDSS, and all other downstream circuit objects in the lateral, such as transformers and loads, are removed from the circuit.

To maintain the equivalence during time-series simulations, there may be multiple equivalent loads created. If each load in the section of the circuit follows the same load profile, there is only need for one equivalent load. For multiple load profiles, or PV output profiles, an equivalent load will be created for each load shape.

Note that with the assumptions of no line charging capacitance or transformer magnetizing current, the sequence-component Norton equivalent is the same as the balanced circuit reduction. Without any shunt terms, the Norton equivalent impedance is infinite, and the loads are moved up to the path. The sequence-component Norton reduction provides equivalent reduced circuit, even with unbalanced current, line mutual impedances, line shunt capacitance, and transformer core losses.

4.4.3 Sequence-Component Load Bus Reduction

The fourth step in the reduction process is to remove buses that are between buses of interest but do not provide critical information. These buses contain loads and are along the path between the substation and the buses of interest. They directly impact the voltages and currents at other buses of interest, but the specific information about voltage is not required for these buses. These buses are reduced using load bus reduction [151].

Load bus reduction is shown Figure 53 for the simplest case with two line sections with impedances Z_1 and Z_2 with loads L_1, L_2, L_3 on each side of the line section. If bus 2 is unnecessary in the equivalent circuit, it can be removed by using (2) - (4) to combine L_2 into L_1 and L_3, resulting in a single line section Z_{eq} and only two loads L_{eq1} and L_{eq2}. The process is repeated any number of times (recursively) to reduce any chain of loads into two buses. Details and mathematical proofs shown in [151] demonstrate that

the load bus reduction method is a fully equivalent circuit with the same total load, voltage drop, feeder impedance, and line losses.

For unbalanced circuit reduction, a 3-phase unbalanced load must be moved to the adjacent buses proportionally to the series impedance, mutual impedance, and the unbalance. This is most easily done using sequence components. Formulas (2) - (4) can be applied to each sequence component individually. For example, the positive-sequence current from the load will be moved to the adjacent buses proportionally to the positive-sequence line impedances. The same process is used for zero and negative sequence. The result is an equivalent circuit with the same phase voltages and phase currents.

For the unbalanced circuit reduction, the sequence-component Norton equivalent created an equivalent fixed-current load and equivalent impedance. The loads are moved using (2) - (4), but in order to perform load bus reduction, the new shunt impedances must also be moved from the bus before it can be removed. The sequence-component Norton equivalent reactors are included in the sequence-component Kron reduction on the diagonals of the Y_{bus} sequence admittance matrix as shunt terms. After Kron reduction, the sum of each row or column is the sequence admittance of the new shunt reactor, with a reactor placed on each of the remaining adjacent buses.

The loads can only be included in OpenDSS as phase loads and cannot be created as sequence current loads. The phase or sequence currents can be converted from one to the other using the conversion matrix *A*, where *a* is a 120 degree phase shift, a=e^(2i*π/3).

$$A = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \tag{34}$$

All loads on the bus are summed together to get the phase current. The total load phase current is converted to sequence currents. The formulas (2) - (4) with sequence

impedances are used to create the sequence currents at the two adjacent buses. Finally, the new equivalent sequence currents are converted back to phase currents to place new loads at the adjacent buses.

If the loads are balanced, the sequence-component load bus reduction is equivalent to the balanced reduction method. Applying the formulas using sequence components allows for reduction of unbalanced circuits and mutual impedance terms. Finally, the sequence-component Kron reduction from step 2 compensates for any shunt terms in the reduction, such as the line charging capacitance and any sequence-component Norton equivalent impedances.

4.4.4 Unbalanced Circuit Reduction Results

The same distribution system used in Section 4.3 is shown below for the unbalanced circuit reduction. In Section 4.3, the feeder was simplified to incorporate all assumptions of no single-phase lines, no single-phase lateral, ideal transformers, and no line charging capacitance. The actual distribution system model with full complexity is shown below to demonstrate the reduction for an actual feeder. The distribution system in Figure 68 can be reduced to only a few buses. During Step 1 of the reduction process, buses 10 and 11 were selected as buses of interest. All other buses in the reduced equivalent circuit are automatically identified as additional buses of interest by the reduction algorithm. Each capacitor bank (buses 5, 6, and 7) must remain in the reduced circuit as a bus of interest to correctly model the reactive power output as well as any capacitor switching. Buses 3 and 4 are identified as necessary to maintain the topology of the reduced circuit. Finally, the transformers between buses of interest (buses 1, 2, 8, and 9) must also remain in the final circuit.

After all buses of interest have been identified, the algorithm begins to reduce the circuit. Before reduction, the distribution feeder contains 1047 lines, 214 transformers, 386 loads, and 1262 buses. After Step 2 of the reduction, the circuit contains 534 lines,

214 transformers, 386 loads, and 749 buses. After Step 3 of the reduction, the circuit contains 92 lines, 2 transformers, 88 loads, and 95 buses. After Step 4 of the reduction, the circuit contains 8 lines, 2 transformers, 10 loads, and 11 buses. As shown in Figure 68, this extremely complex system can be reduced to a simple circuit with only a few parameters that wholly and accurately represents the currents and voltages at all buses of interest in the equivalent circuit.

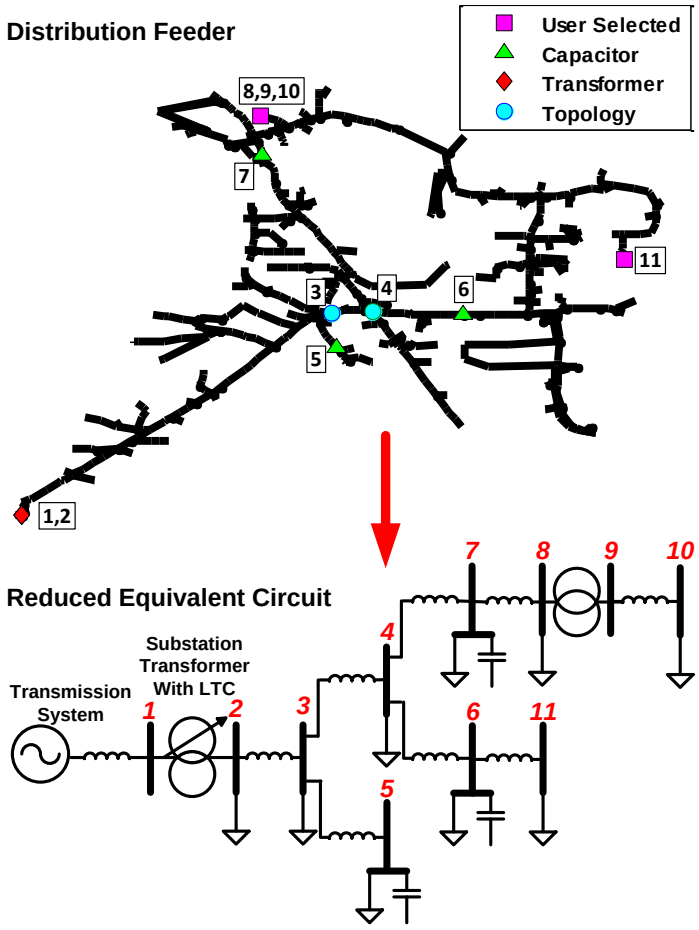


Figure 68. A full distribution system feeder reduced to a simple equivalent representation.

When looking at the voltage profile of the feeder, there are now different voltages on each phase. Figure 69 shows the voltage profile of the full distribution feeder model during the circuit reduction process with the phase voltages A, B, and C signified with the colors black, red, and blue respectively. These four figures show that during the

reduction process, the complexity of the circuit is reduced considerably during each step. However, despite this reduction, the accuracy of the voltage profile at the buses of interest remains unaffected. The reduced circuit also maintains all distances, short circuit currents, and impedances between buses of interest. During the reduction, all other complexity and bus voltages in the original circuit are lost. This is advantageous if the distribution engineer is not interested in the voltage at those thousands of other buses. If the information or characteristics of a bus are desired, it can simply be selected as a bus of interest before reduction.

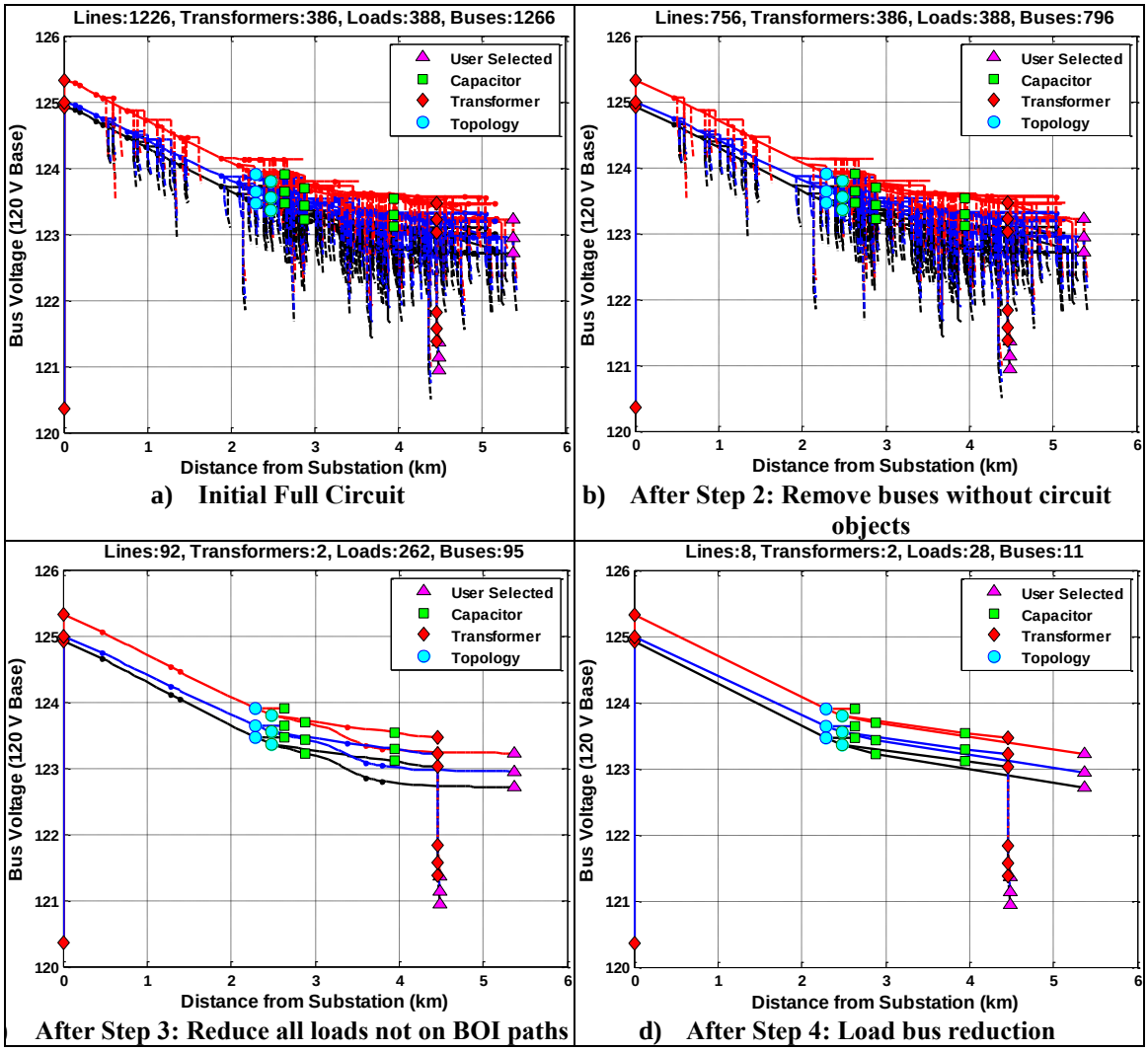


Figure 69. Feeder voltage profile plot a) before circuit reduction, b) after sequence-component Kron reduction, c) after sequence-component Norton equivalent, and d) after load bus reduction. Phase voltages A, B, and C are signified with the colors black, red, and blue respectively.

The equivalence of the reduced circuit to the full circuit is analyzed by comparing the voltages for the snapshot simulation shown in the voltage profile plots in Figure 69. The differences for the power flow solution bus voltages are shown in Table 12. The error is generally in the order of 10^{-6}. This error is likely due to small rounding differences in the reduction process, and differences of 0.000001 are small enough to be insignificant during the interconnection process.

Table 12. Snapshot Analysis of Voltages for Buses of Interest

Bus	Full (kV)	Reduced (kV)	Difference (pu)
1	115.344733	115.344733	-0.911 E-07
2	20.638734	20.638734	-1.108 E-06
3	20.406465	20.406465	-2.461 E-06
4	20.389497	20.389497	-2.485 E-06
5	20.404767	20.404767	-2.479 E-06
6	20.368781	20.368781	-2.555 E-06
7	20.346952	20.346952	-2.464 E-06
8	20.334235	20.334235	-2.458 E-06
9	0.4863754	0.4863754	-2.458 E-06
10	0.4845656	0.4845656	-2.458 E-06
11	20.288699	20.288699	-2.878 E-06

It is interesting to compare the error for the unbalanced circuit reduction to the balanced method. The same circuit and buses were used in [152] for balanced reduction. In this previous work, all loads were made to be balanced three-phase, line shunt capacitance was removed, and transformers did not have any core losses. In general, the feeder was assumed to be quite simplified and unrealistically ideal. The errors from [152] are shown in Table 13 compared with the errors for the new unbalanced circuit reduction of the full unbalanced feeder model. The balanced circuit reduction was shown to be mathematically equivalent in [151] and produced slight simulation errors up to $5.8*10^{-6}$. The unbalanced circuit reduction can also be said to be fully equivalent with errors up to $2.9*10^{-6}$.

Table 13. Comparison of Errors for Balanced Circuit Reduction on a Manufactured Ideal Balanced Circuit Vs. Errors for an Unbalanced Circuit

Bus	Balanced Difference (pu)	Unbalanced Difference (pu)
1	1.04E-06	-0.911 E-07
2	1.19E-05	-1.108 E-06
3	2.06E-06	-2.461 E-06
4	1.14E-06	-2.485 E-06
5	2.04E-06	-2.479 E-06
6	-3.00E-07	-2.555 E-06
7	-3.42E-07	-2.464 E-06
8	-4.82E-07	-2.458 E-06
9	-4.66E-06	-2.458 E-06
10	-5.80E-06	-2.458 E-06
11	4.80E-07	-2.878 E-06

In order for the reduction method to be truly valuable in improving efficiency, it must maintain its effectiveness and accuracy for timeseries simulations. The timeseries validates the equivalence of the reduced circuit in a much more accurate way, because as the load varies through time, the losses are a squared term and nonlinear. A reduced circuit could result in the same power flow solution for one load level without being equivalent through time, compensating for losses and voltage regulation equipment switching. The reduction was validated by simulating the peak-load week for both the full and reduced feeder. The bus voltages at the user-selected buses (bus 10 and bus 11 in Figure 68) were monitored and recorded during both runs. The phase-average voltages for each bus during the full and reduced circuit simulations are shown in Figure 70. The resulting error in per-unit voltage can be seen in Figure 71.

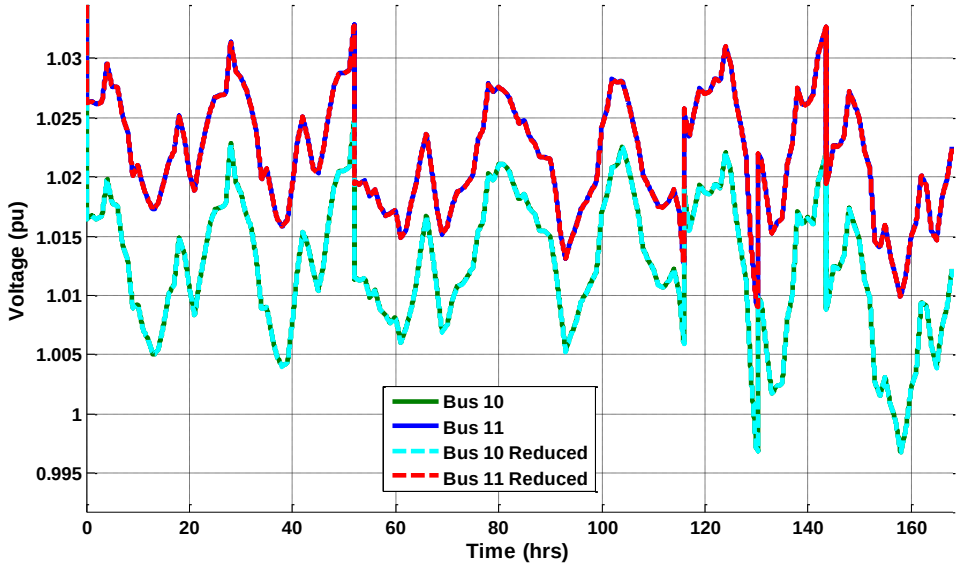


Figure 70. Average bus voltage during one week time-series simulation

As shown Figure 70, the error is not visible given that is on the order of 10^{-5} or 10^{-6}. Figure 71 shows that the error typically only varies by less $3x10^{-6}$ V_{pu}. There are two exceptions around hours 130 and 143. These error deviations are a result of the LTC switching. Because the simulations were run at a 1-minute resolution, the 1 minute difference in switching time between the full and reduced simulations results in a larger error. This error would be reduced for higher simulation resolutions. The key point is that the error does not change significantly with the load level. The load varies to less than 50% of its peak, but the error only changes very slightly through time, almost independently from the load profile.

Another noteworthy attribute of this plot is the vertical resolution in the error as it steps from one error value to another. This is because the data returned by the simulation only has an accuracy of 1 mV. After converting to per-unit, this resolution is $3.61x10^{-6}$ V_{pu}, which is the size of the vertical steps. Note that the error from the circuit reduction is very much on the order of the resolution of the power flow solver. This difference between the full and reduced circuit can be attributed to some rounding errors.

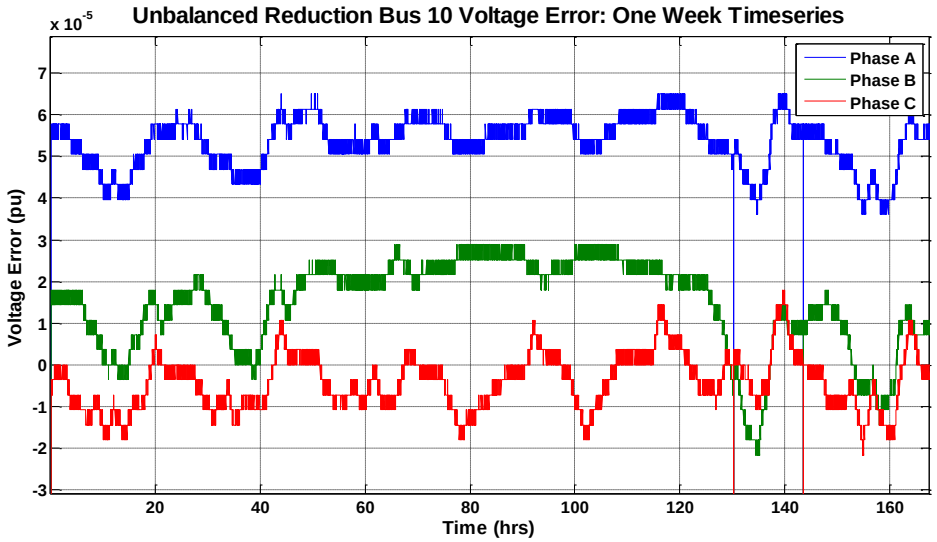


Figure 71. One week timeseries error of bus 10 per-unit voltage

The algorithm presented in Section 2 and in previous work can be applied to single-phase buses of interest. The reduction methods can be used either on unbalanced 3-phase line sections or single-phase sections. The only change to the algorithm is that a bus where the change in number of phases occurs must remain in the reduced circuit as a topology bus. The algorithm automatically identifies this necessary bus by finding the first 3-phase bus upstream of the single-phase bus of interest. To demonstrate the method, bus 12 was selected by the user at the end of a single-phase section on B-phase, as shown in Figure 72a. Bus 13 was automatically identified as a topology bus of interest because it is the split from the path of other buses of interest 4 and 7. Additionally, Bus 14 was automatically identified as a topology bus of interest because it is the bus where the number of phases changes.

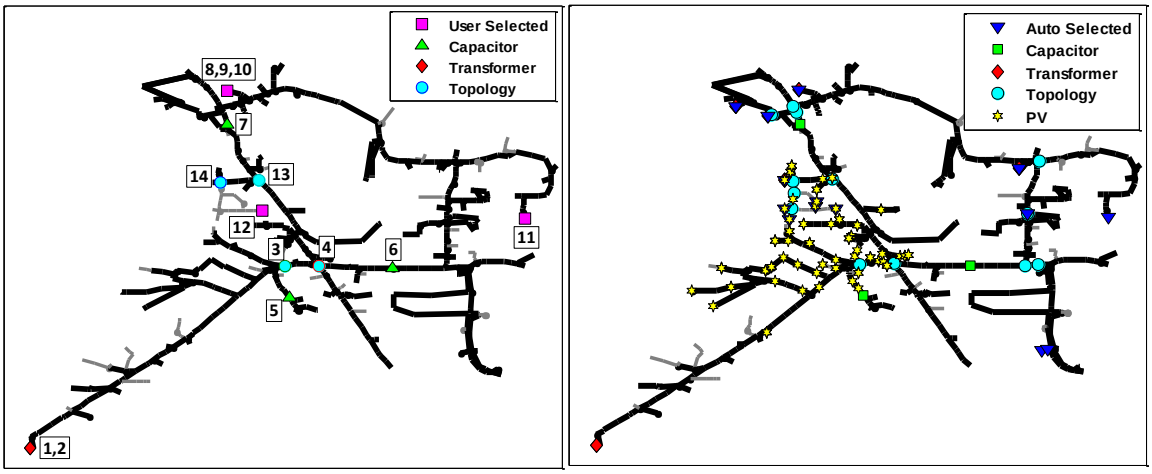


Figure 72. Example feeders for a) single-phase bus of interest (bus 12), and b) distributed PV systems

This circuit was validated to have very little error, similar to the previous example, of approximately $3*10^{-6}$ V_{pu} error from the full circuit power flow results. The voltage profile for the full circuit and reduced circuit are shown in Figure 73 along with the number of lines, transformers, loads, and buses in each model.

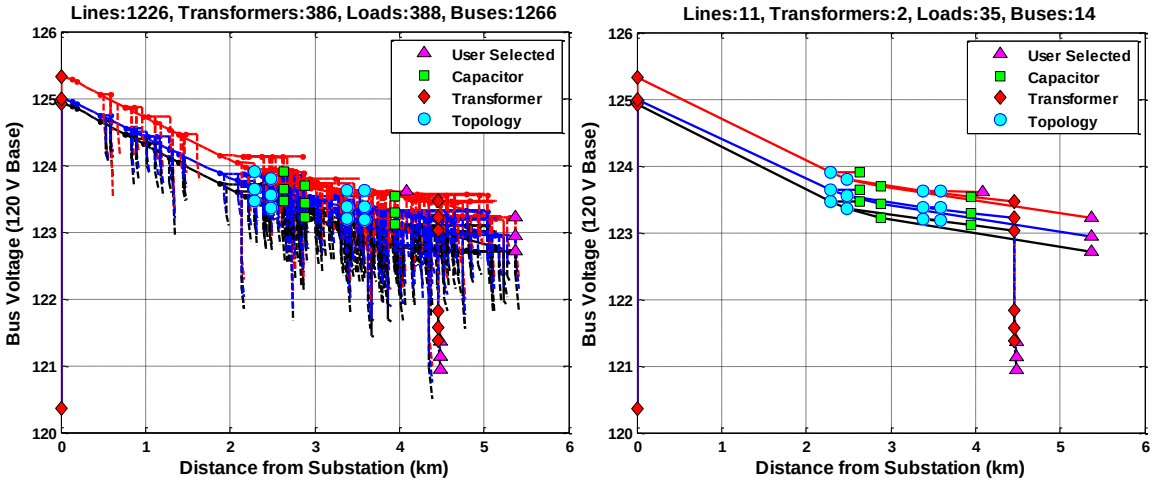


Figure 73. Voltage profile for a) the full circuit and b) the equivalent reduced circuit.

The unbalanced circuit reduction methodology can also be applied to distributed PV. A total of 7.5 MW of PV was distributed around the center of the feeder, as seen in Figure 72b. The PV systems are a mix of single and three phase systems. Buses of

interest were automatically selected by the algorithm discussed in Section 4.5 to add the end of lines and the low/high voltage buses.

The feeder voltage profile for the full circuit and reduced circuit is shown in Figure 74. The number of buses has been reduced to 3.4% of the original number, while maintaining the accuracy. The largest voltage error between the full and reduced circuit for any of the buses of interest is $2.1*10^{-6}$ pu.

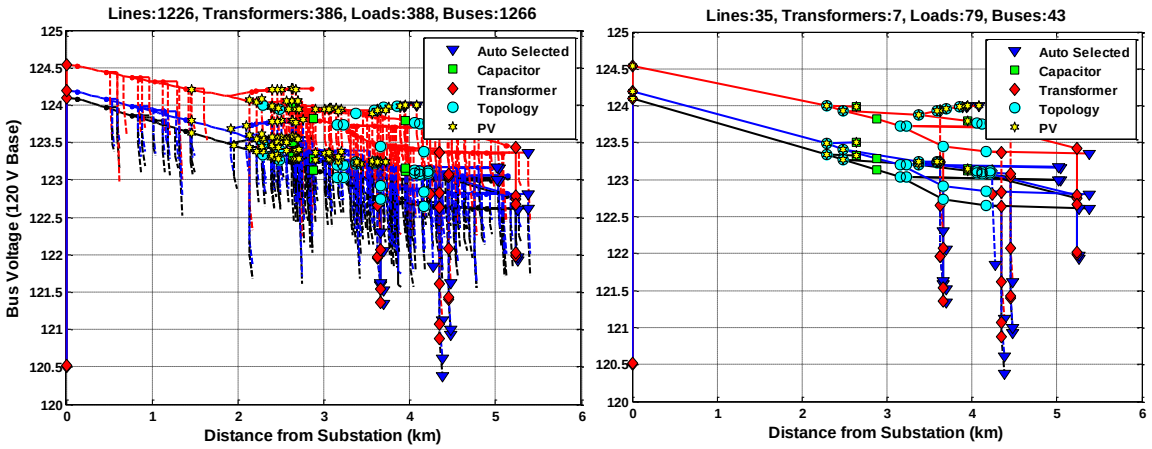


Figure 74. Feeder voltage profile for the full circuit and the reduced circuit.

The circuit reduction methodology was expanded to simplifying unbalanced feeders with shunt components, while maintaining the accuracy and the feeder topology of the full model. The accuracy of the method was shown for a snapshot simulation and a timeseries simulation with the error in the order of 10^{-6}. The method was also demonstrated with a single-phase user-selected bus of interest and distributed PV.

The magnitude of reduction for the unbalanced circuit reduction is the same as the unbalanced circuit reduction with the number of buses and lines at approximately 1% of the number of the full circuit. The only cost of the unbalanced circuit reduction is few more components at the remaining buses compared to the balanced reduction method. Due to unbalanced, each bus must contain 3 single-phase loads at each bus instead of one balanced 3-phase load. The core losses of the service transformers and the line shunt capacitance have also been grouped into a single impedance value at each bus in the

reduced circuit. The overall accuracy and reduction magnitude has been maintained while accounting for unbalanced current, shunt capacitance, and transformer losses.

4.5 Automatically Detecting Buses of Interest

Detecting the required buses or interest (capacitor, regulators, topology buses, etc.) that were presented in the previous sections is straight forward. If only the bare minimum of required buses of interest are used, the circuit generally reduces to a very small number of buses, likely around 10 buses. Adding any additional buses that should remain in the reduced circuit beyond the required buses is determined by the buses that the user selects. This section discusses a few methods to automatically detect some buses that may be of interest, but are not required to maintain the equivalence. The concept is to help the user select the best buses automatically and consistently. New intelligent algorithms have been developed to select buses of interest to better characterize the feeder as a whole.

Adding certain key buses can be as simple as setting up a threshold of adding any bus with a large (>100kW) load or generator connected to it. Voltage thresholds can also be set to keep the lowest voltage buses or highest voltage buses that also have PV. One of the most interesting developments in detecting buses of interest is selecting end of feeder buses that can be used to show the main topology and layout of the feeder. An algorithm was developed to identify the ends of 3-phase lines and to add them to the buses of interest. All 3-phase ends of lines where there is a 3-phase line coming into the bus but no other 3-phase medium-voltage line coming out of the bus are identified. The farthest 3-phase bus is first identified, and the path between that farthest 3-phase bus and the substation is drawn. Any of the previously identified 3-phase ends of lines that are within a certain conductor length to any bus on the path are discarded. This removes any short laterals that are not necessary to classify the topology. Next, a recursive algorithm is implemented that selects the farthest 3-phase end of line in the remaining list, adds this

bus to the buses of interest, adds the path between the newly selected 3-phase end of line and the substation, and discards any 3-phase end of lines within a certain distance to paths between the selected end of lines and the substation. The distance threshold can be a specific distance, a percent of the total feeder length, or selected by the user.

The method is demonstrated below for ML1, with the full circuit shown in Figure 75. The reduced circuit for when no buses are selected and only the buses of interest required to maintain equivalence are included is shown in Figure 76. Figure 77 demonstrates the case where the lowest voltage buses are automatically selected as buses of interest. Using the recursive algorithm to detect certain key end of line buses, the circuit is reduced to Figure 78. Finally, selecting both the low voltage buses and end of line buses in the auto-selection results in Figure 79.

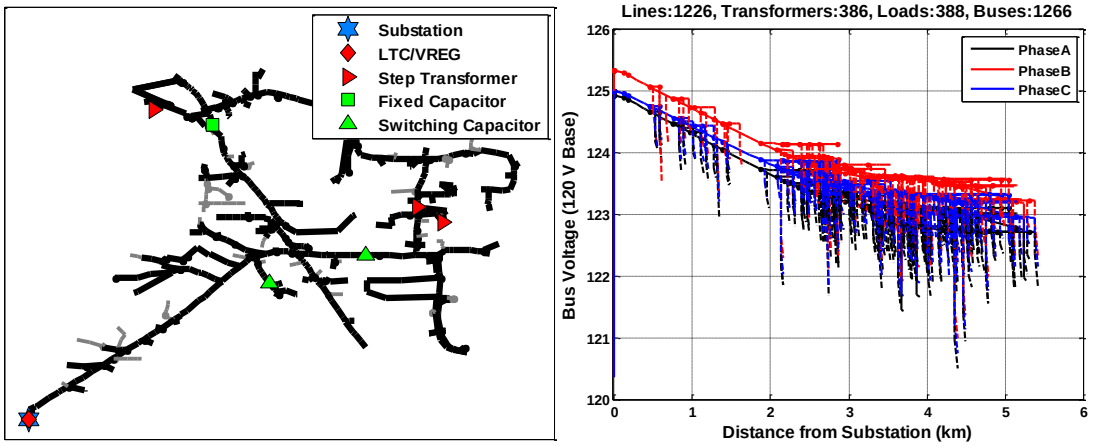


Figure 75. The full model for feeder ML1

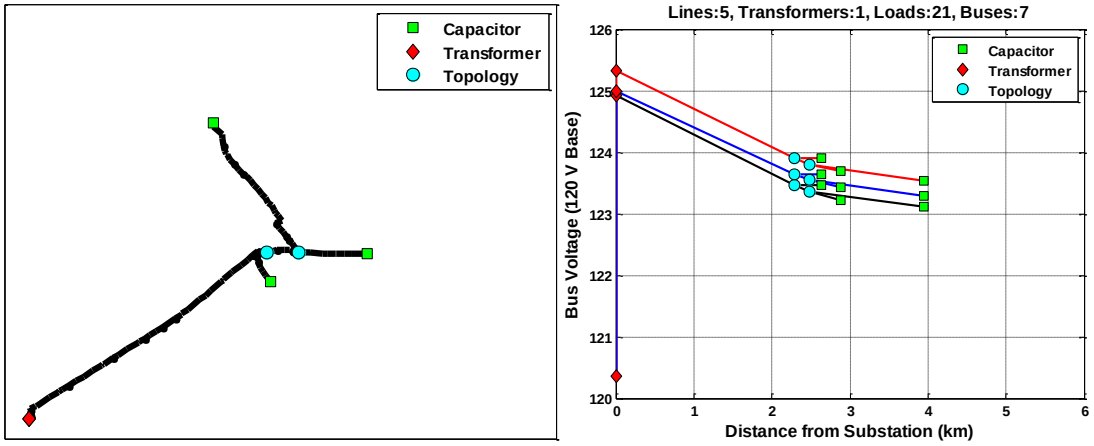


Figure 76. Feeder ML1 reduced circuit with no selected buses of interest.

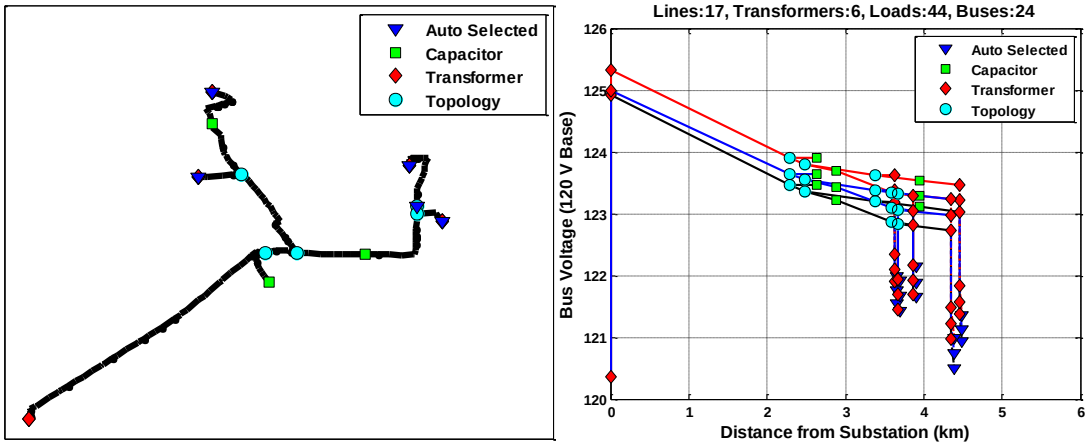


Figure 77. Feeder ML1 reduced circuit with low voltage buses added.

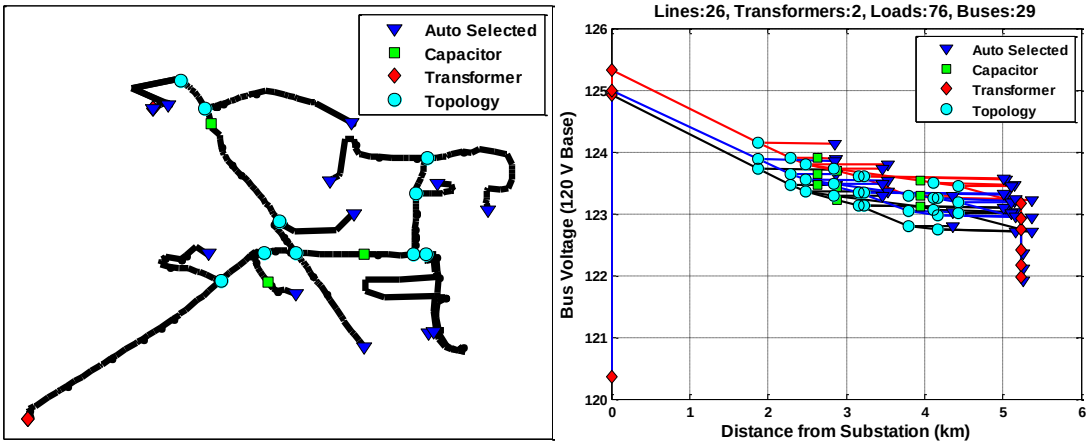


Figure 78. Feeder ML1 reduced circuit with end of line buses added.

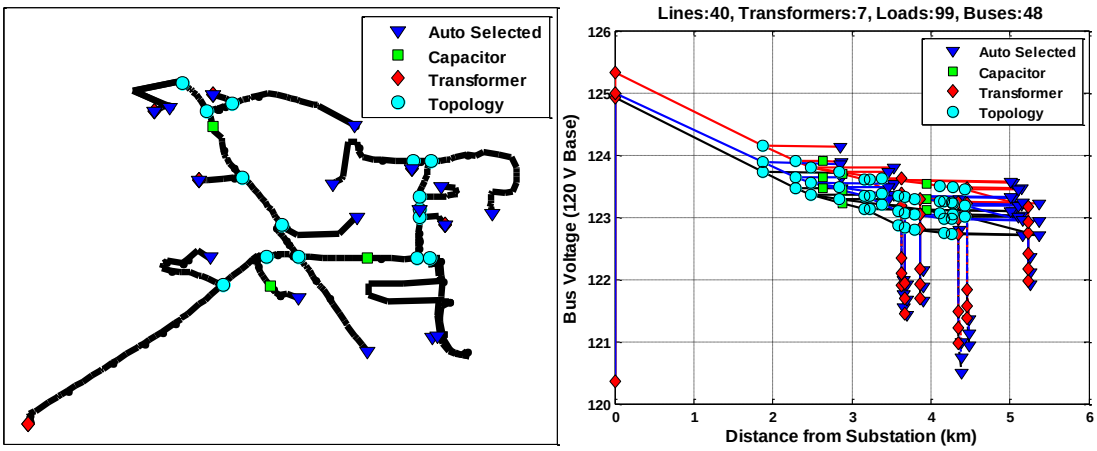


Figure 79. Feeder ML1 reduced with low voltage and end of line buses added.

4.6 Reduction Results for Several Feeders

In order to demonstrate that circuit reduction can be applied for a range of feeder topologies, five different distribution systems have been reduced. Each of the feeders is a real feeder that has been modeled with the full complexity. The resulting high level of accuracy for each of the reductions proves that the methodology is valid for a range of load levels, conductor types, feeder sizes, topologies, voltage drops, and power factors. The full model and reduced model are shown for each feeder in Figure 80 through Figure 84. In each case, the algorithm was set to automatically select some buses of interest for end of feeder buses and low voltage buses. Table 14 includes the percent reduction for how many of the buses were removed, along with the maximum error for any phase voltage at buses of interest between the full and reduced models.

Table 14. Circuit Reduction for Five Feeders.

Feeder	Percent Reduction	Maximum Voltage Error from Full Model
UD11	96%	<0.02%
ML1	98%	<0.01%
UT11	96%	<0.01%
Ckt7	98%	<0.02%
UQ11	97%	<0.02%

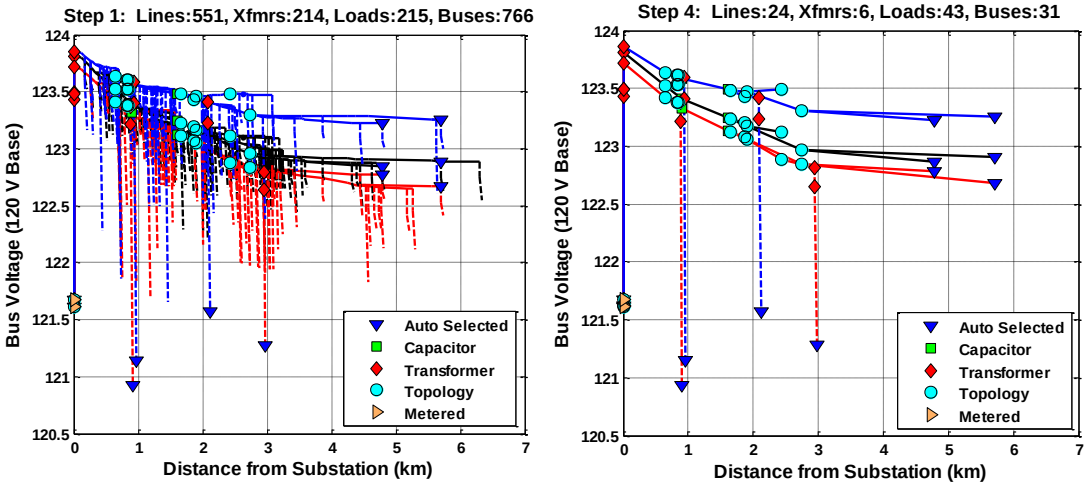


Figure 80. Feeder UD11 full and reduced model.

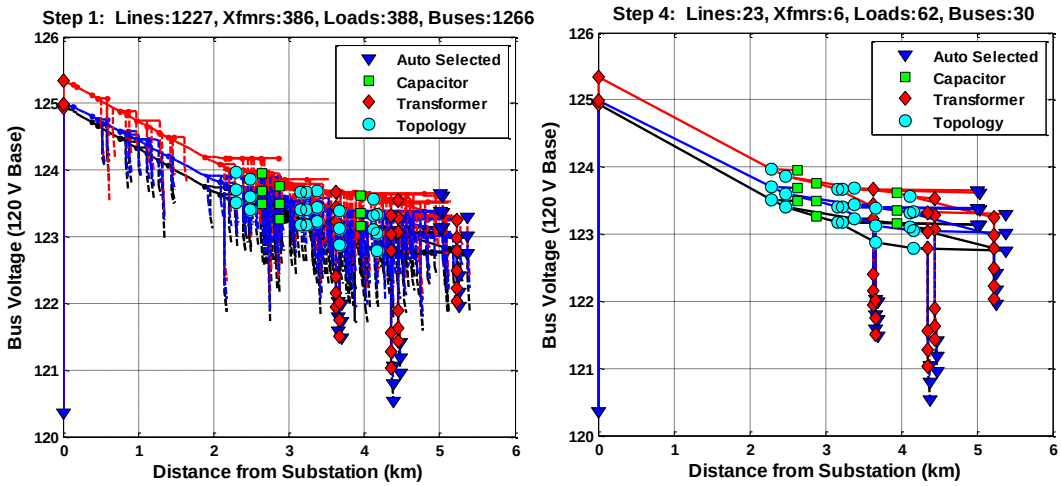


Figure 81. Feeder ML1 full and reduced model.

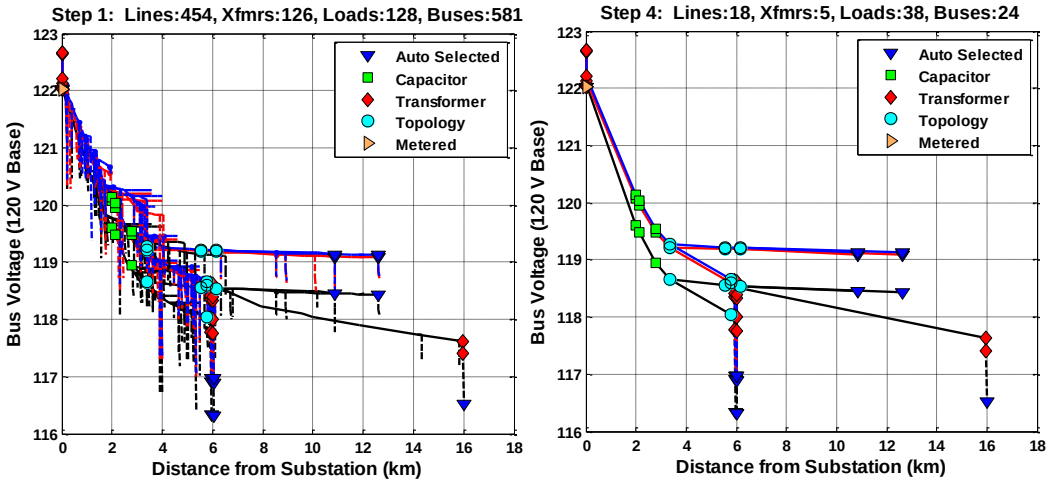


Figure 82. Feeder UT11 full and reduced model.

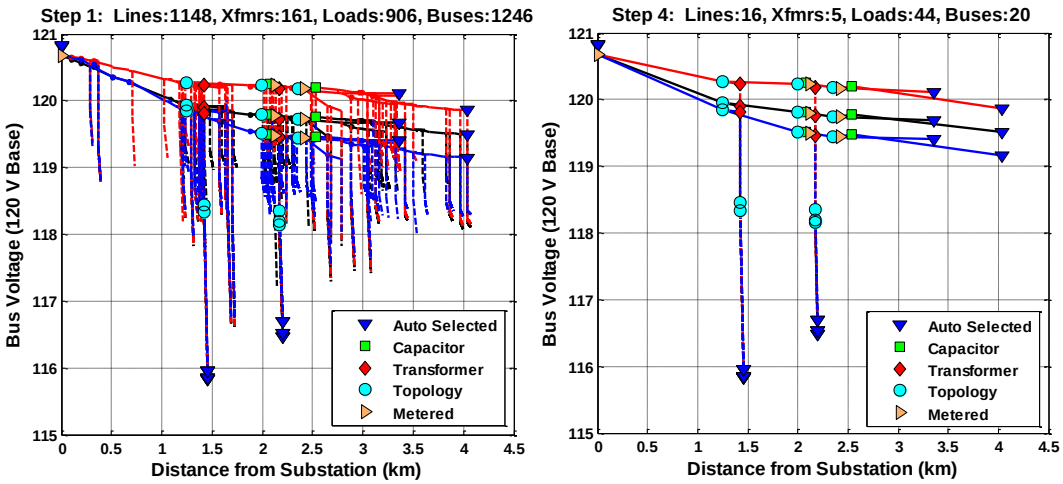


Figure 83. Feeder Ckt7 full and reduced model.

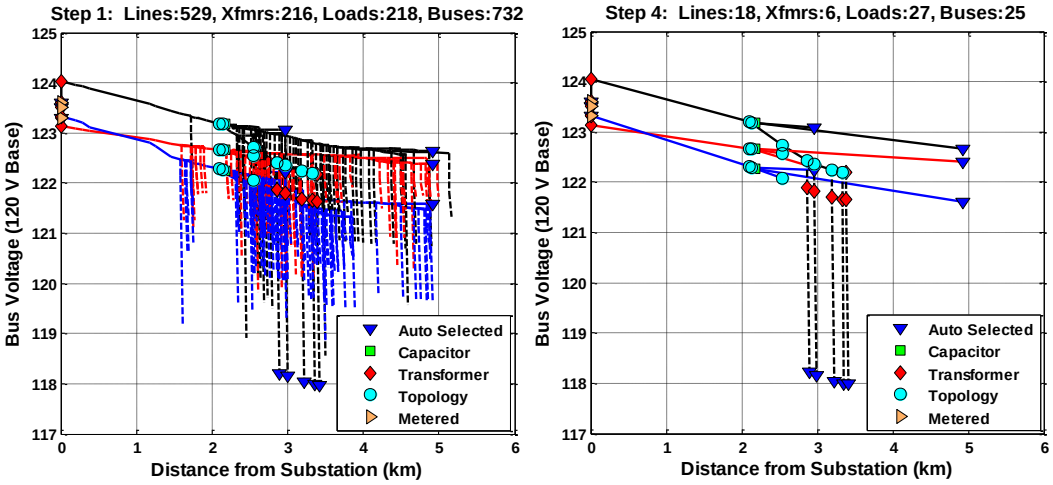


Figure 84. Feeder UQ11 full and reduced model.

CHAPTER 5: ADVANCED SIMULATION METHODS FOR PV INTERCONNECTION ANALYSIS

5.1 Introduction

This section discusses novel methods for analyzing PV interconnections with advanced simulation methods. The focus is feeder and location-specific impacts of PV that determine the locational PV hosting capacity. EPRI has performed significant research in the area of feeder hosting capacity for PV [84, 85]. While their research was focused on determining the hosting capacity for the entire feeder, this research expands the idea to investigate individual areas of the feeder to determine the local maximum. In this analysis, the impact on maximum feeder voltage caused by connecting a range of PV sizes on various buses is shown, along with the effect of these installations on line loading and feeder violations. The detailed analysis is performed on 50 different real distribution systems in order to study the variations in PV locational hosting capacity caused by different circuit characteristics.

5.2 Interconnection Location Analysis

This section presents the foundation for the methodology of analyzing PV interconnection on the distribution system by size and location. The concepts are presented for simulating large numbers of potential PV interconnection locations and sizes in order to determine the locational (distance, impedance, and conductor type) limitations. These concept and the algorithms are developed more in later sections.

The circuit used for this initial analysis is EPRI test circuit 7 (Ckt7) available online at [135]. The topology of this feeder can be seen in Figure 85. The feeder is a short (4 km), 12.47 kV feeder with mostly industrial customers. This feeder has 288 buses on the medium-voltage 12.47 kV system, 200 of which are three-phase. For voltage

regulation, Ckt7 has two switching capacitors but no load tap changer (LTC) at the substation or voltage regulators in the feeder. The substation transformer includes 14 feeders and is connected to a strong, 115 kV transmission system. The full-load demand at the substation is 36,111 kVA at 0.95 lagging power factor. The feeder loads use a conservation voltage reduction (CVR) load model that changes the power slightly based on the voltage, using values of 0.8 for real and 3.0 for reactive power [150].

To examine the impact of central PV installations on the feeder, an extensive process is used to step through all considered locations, storing data from the power flow solution for each scenario. The set of scenarios include a significant range of system sizes and locations. Due to the fact that Ckt 7 is an industrial feeder, the focus of the analysis is on single, large-scale, central PV plants. The PV systems were sized ranging from 0 to 10 MW in 100 kW increments, and all three-phase buses were considered. For each of the 100 considered system sizes at each of the 200 three-phase buses, a total of 20,000 snapshot power flow simulations were performed. Each power flow simulation is performed in full detail for the distribution feeder with hundreds of components, complex voltage regulation controls, and feeder loads allocated on the secondary system at the end of triplex lines. The unbalanced three-phase power flow is solved using the distribution system software OpenDSS [117] with GridPV [121] to perform analysis in MATLAB. During each power flow simulation, the maximum per unit bus voltage on the feeder is recorded, along with the maximum line loading (line current/line rating) of all lines. The solutions from the power flow simulations for each PV study case are analyzed to determine any violations or limitations in the distribution system that would not allow the particular interconnection. Initially, fixed power factor PV systems producing only real power are considered as they are most common [153], but future work will consider active voltage control [154].

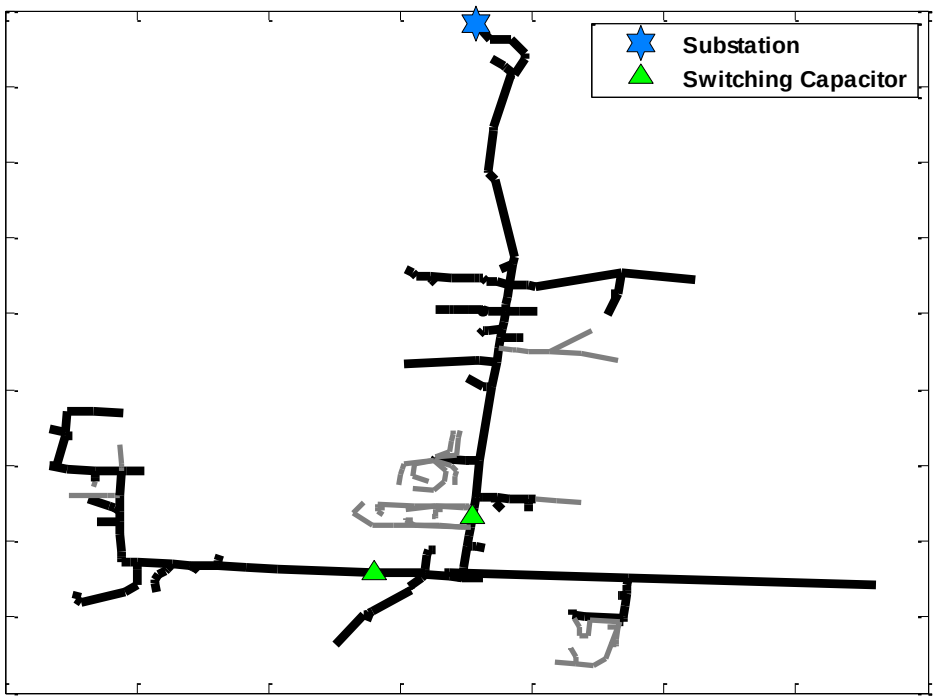


Figure 85. Ckt7 Topology and Voltage Regulation – black lines indicate three-phase.

The same three-phase buses were iterated through to determine the maximum allowed PV system size before resulting in an over-voltage violation or a line over-loading anywhere on the feeder. Voltage violations are classified as anything outside of Range A of ANSI C84.1 [134], and the line over-loading threshold is set at 100% of the normal line rating. Each bus was considered individually to find the maximum possible PV size, with a 50 kW resolution, before a violation occurs. Figure 86 shows a flow chart of the methodology employed for this analysis.

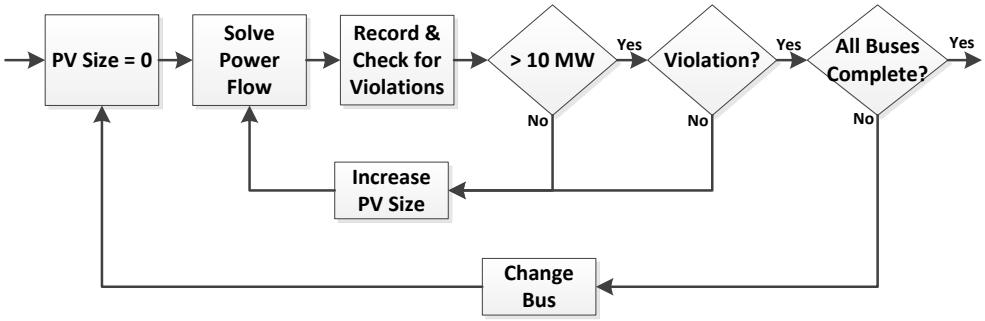


Figure 86. Flow chart of methodology.

For each scenario, the worst case is simulated with the PV system outputting rated power at unity power factor. Various magnitudes of feeder load were considered. It was found that over the year, the minimum daytime (9 am to 3 pm) load is approximately 40% of the feeder peak load, and the average daytime load is 61% of the feeder peak. The daytime load is less than 50% of the feeder peak only 17% of the time, so the minimum load considered is 50%. The maximum load considered is 100%. Together these two scenarios respectively represent the worst and best case scenarios for connecting a system with rated output to the feeder.

Maximum bus voltage was the first attribute examined in the analysis. Figure 3 shows the distribution of the maximum bus voltage due to installing a central PV system at various locations for the 50% load case as PV system size increases from 0 to 10 MW. To reiterate the methodology and how this graph was obtained, there is data for every 0.1 MW step along the x-axis for system sizes ranging from 0.1 MW to 10 MW. For each of these PV system sizes, there are 200 scenarios with power flow solutions, corresponding to each of the three-phase buses, which consider each of the possible interconnection locations. For each of these scenarios, the maximum bus voltage on the feeder (in pu) was found. The combination of these 200 points for each of these 101 system sizes (including base case 0 MW) yields the distribution shown. For example, consider the case of a 10 MW PV system. For this system size, approximately 25% of the 200 potential three-phase buses will result in a max bus voltage above 1.05 pu. Therefore, for a 10 MW central PV system on Ckt 7, there are 150 buses at which this plant can be connected that will not result in an over-voltage violation given 50% load and rated PV output.

It is important to note that Figure 87 is the maximum voltage anywhere in the feeder. There is a clear point around 1.3 MW below which any interconnection of central PV will not cause a PCC voltage to be larger than the substation; therefore, the highest voltage occurs near the substation. As the PV size increases above this point, more interconnection locations will have PCC bus voltages that are larger than the substation,

depending on their distance from the substation. Buses furthest from the substation will deviate first. These further buses will have PCC bus voltages that increase at a faster rate with increases in system size, as illustrated by the increasing spread among the percentiles. The median maximum bus voltage does not surpass 1.05 pu at 10MW. However, line thermal limits make any analysis of larger systems impractical.

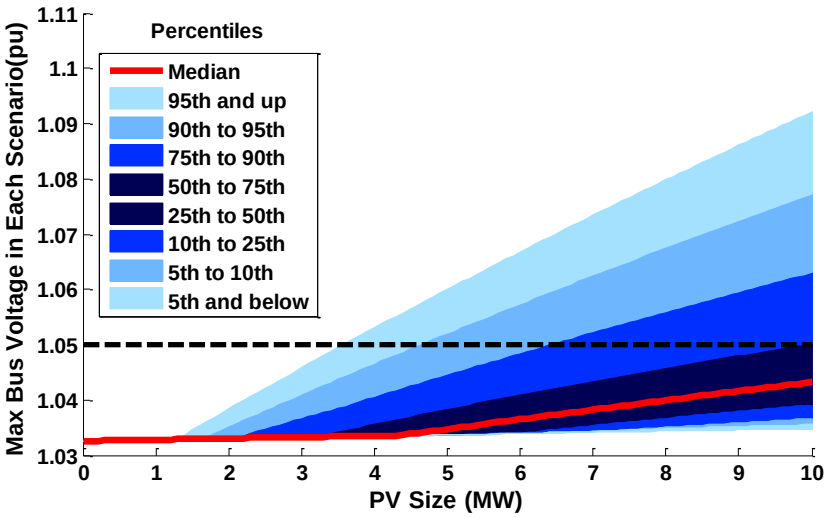


Figure 87. Effect of PV size on max bus voltage under 50% load.

The plot from Figure 87 was replicated for maximum line loading and is shown in Figure 88. The maximum line loading for each of the 200 interconnection locations was determined considering each of PV system sizes. The impact on line loading is significantly more clustered than the impact on bus voltage. For example, when considering a 3.5 MW system, none of the scenarios result in over-loading. However, when considering a 3.9 MW system, over 50% of the scenarios result in over-loading. This is due to distinct cable types used throughout a feeder. A given distribution system generally only has a few different cable sizes. In this case, all three-phase laterals have the same line rating and overload at the same time.

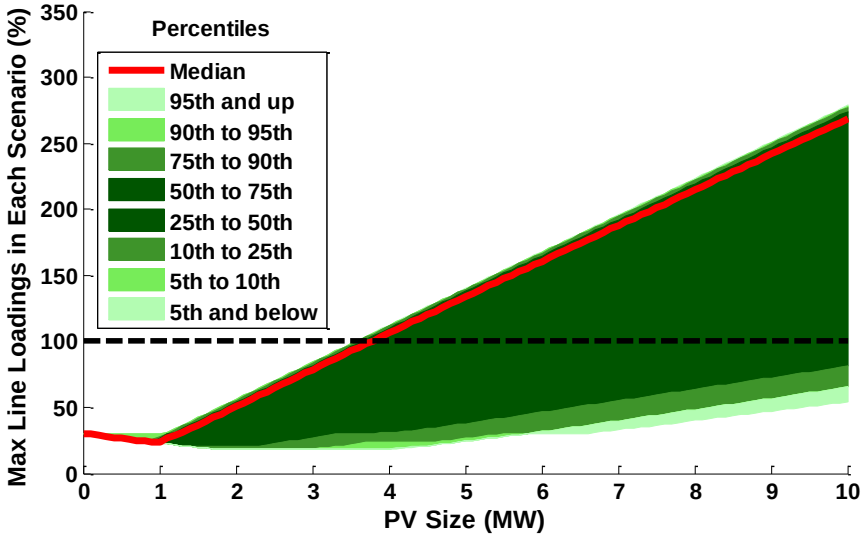


Figure 88. Effect of PV size on max line loading under 50% load.

The same data used for Figure 87 was analyzed using the distance of the PV interconnection to the substation as an independent variable in Figure 89. Each data point in Figure 89 represents a power flow solution with the maximum bus voltage plotted as a function of this distance and colored to indicate the PV system size. Figure 89 validates the difference in slopes between percentile ranges in Figure 87. Interconnections toward the end of the feeder exhibit a wider range of maximum voltages, and therefore a larger response to differences in system size. The feeder backbone is clearly noticeable towards the bottom of Figure 89. On the backbone particularly close to the substation, increases in system size have a relatively small effect on the PCC bus voltage. System size exhibits less impact on these buses than it does on other buses with higher impedances between the PCC and the substation. For these buses on the backbone and close to the substation (less than 0.5 km), the highest bus voltage will be that of the substation. The increase in maximum voltage for these cases is not due to the PCC bus voltage, but rather an increase in substation voltage due to the marginal decrease in load being served by the substation.

However, when the PV is further away from the substation on the feeder backbone, the increased resistance causes the impact of system size on PCC bus voltage

to increase. This results in the linear trend at the bottom of the graph from 1 km to 2.5 km shown by the dark red points indicating a 10 MW system size, which indicates a larger maximum bus voltage for the same system size. There is also some deviation from this linear trend. This is due to the higher impedance laterals that separate from the backbone relatively close to the substation. These higher impedance laterals have a distance to the substation equivalent to other locations that are downstream on the backbone, but their increased resistance causes the system size to have a greater impact on their PCC bus voltage.

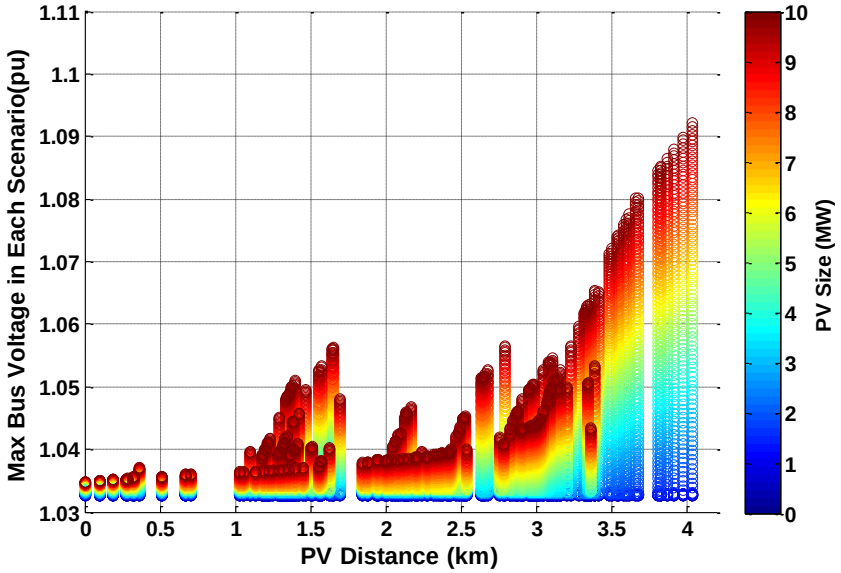


Figure 89. PV size and distance effect on max bus voltage under 50% load.

Given this impact of PCC impedance to the substation, the same data was analyzed using impedance as well as PV system size as the independent variables in Figure 90. As expected, this creates a smooth relationship for most of the region. However, differences in the load sizes downstream from the PCC bus causes the irregularities observed up to around 0.7 Ω. A PCC bus with larger downstream load will, in the base case, have a lower voltage than another PCC bus with the same impedance but less downstream load. As PV system size is increased, the impact of the system size on each PCC voltage will be the same, with the voltages differentiating by this initial

discrepancy. A PCC bus with larger downstream load will always have a lower PCC bus voltage for a given system size than will a bus with larger downstream load. Therefore, the maximum bus voltage will be the substation voltage more often for cases with large amounts of downstream load.

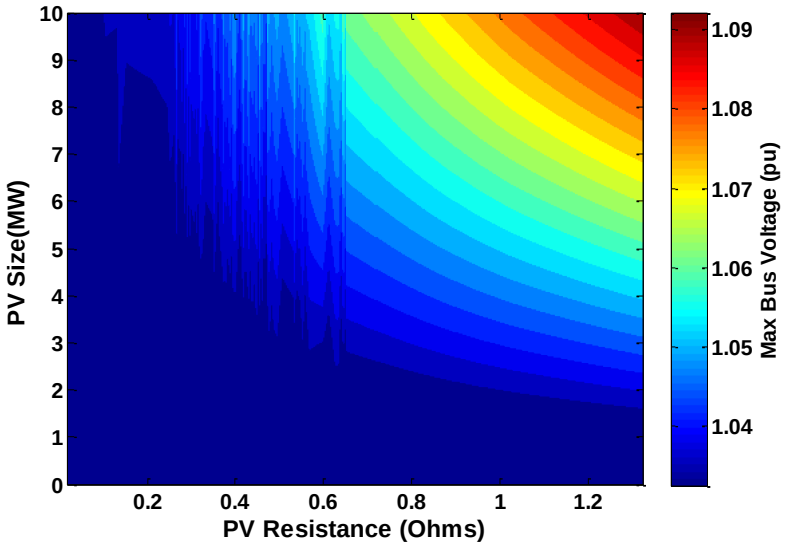


Figure 90. Max bus voltage as a function of PV size and resistance under 50% load.

5.3 Locational Hosting Capacity

After analyzing the effect of PV system size on bus voltage and line loading separately, it is useful to observe the effect in terms of overall violations. Figure 91 shows the percentage of locations for a given PV size that result in any violation, either over-voltage or line-loading, as PV system size is increased. The results are also shown for only considering over-voltage violations and only considering line-loading violations. Around 3.6 MW there is a drastic increase in any violations from zero violations to over 50% of the considered scenarios at 3.9 MW. This is due to how similarly the line loading profiles increase together and was mentioned in the discussion of Figure 88.

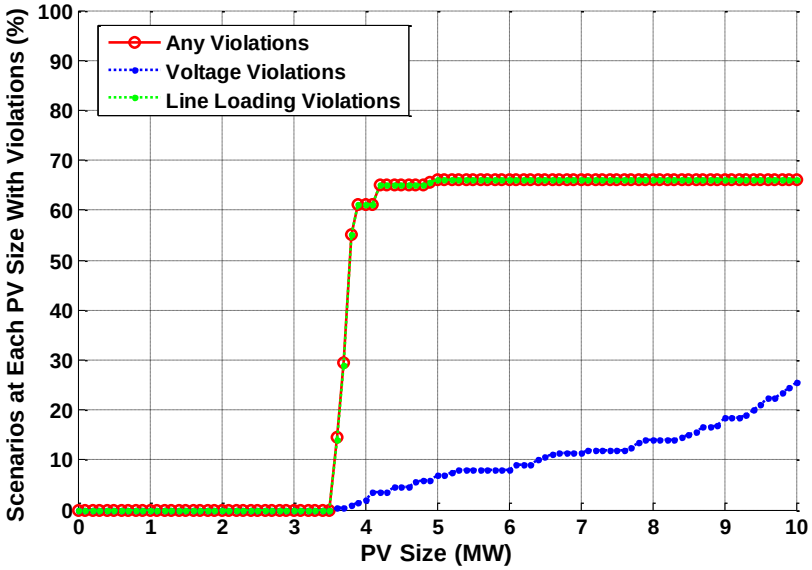


Figure 91. Percent of PV scenarios at each PV size with violations under 50% load.

After observing the effect of PV system size on scenario violations, the maximum allowed system size is investigated for each of the 200 PCC buses before a violation occurred for both the half-load and the peak-load cases. The maximum possible PV system sizes are plotted on the circuit topology, shown in Figure 92, varying both marker size and color to correspond to relative maximum system size.

This clearly shows the PCC locations that are causing the line-loading violations and the large disparity between allowed system sizes on the backbone versus that of the laterals. However, these figures also show an interesting similarity: there is little difference when considering the half-load and the peak-load case between the maximum allowed PV system size on a bus. When the load is doubled the maximum PV system size allowed on the feeder increases 8.4% from 14.95 MW to 16.2 MW. The average increases 4.6% from 6.55 MW to 6.86 MW. Because the limit for maximum PV system size allowed is generally a result of the line ratings on this feeder, the change in allowed PV size under different values of feeder load is a function of the downstream load. For example, the change in current flow through a lateral is similar for different load magnitudes, so the maximum allowed PV system size has little change.

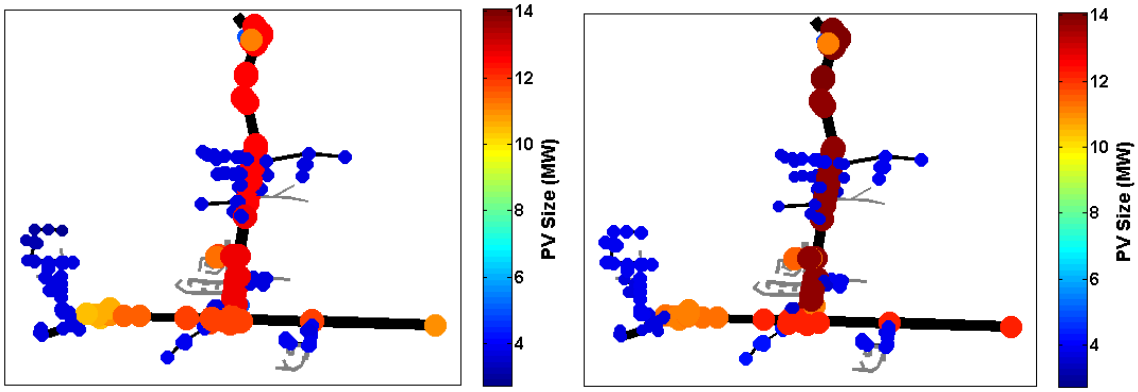


Figure 92. Maximum allowed PV size at a single bus at A) 50% load, B) peak load.

This research developed a method to analyze the impacts of a central PV system on various locations of a feeder for multiple PV system sizes and feeder loads. It was found that for the example feeder Ckt7, the size of the PV plant, regardless of location, is mostly impacted by thermal limits as opposed to voltage limits. For this feeder, the feeder load has little impact on the allowed system size before these thermal violations occur. With regard to voltage violations, the biggest factor is impedance from the PCC to the substation. The location of PV on the feeder, because of its impact on impedance to the substation, will affect the rate at which an increase in PV size increases PCC voltage.

5.4 State of Voltage Regulators and Capacitors

In the previous analysis for Ckt7, there was no voltage regulation equipment. In this section, the analysis methodology is expanded to include voltage regulation equipment, such as substation load tap changers (LTC), line voltage regulators (VREG), and switching capacitors. The developed methods consider and test the range of potential states that are within the control limits of the regulators and capacitors.

For stochastic steady-state simulations, the actual system state (regulator tap position and capacitor connection) is unknown and could be in several different but

equally likely states. This is due to the fact that all voltage regulation equipment (LTC's, VREG's, switching capacitors) have a voltage regulation setpoint and a voltage band around this setpoint, which are set to maintain the voltage within the voltage band. To prevent an excessive number of operations for the physical hardware that contributes to degradation and wear, the bands on the voltage regulation equipment are set to be fairly large. Having a large regulation band also helps prevent the hardware from nuisance changes, which are when the voltage regulation equipment operates only to have to operate again because the initial operation was over-corrective. If several voltage regulators are in series with each other along the feeder, the regulation band provides a buffer so that every time one regulator changes taps, every other regulator in the series does not also have to change taps.

The presence of the voltage regulation bands means that a given power flow can have several solutions, each equally valid depending on the states of the voltage regulation controls. For example, consider the most common voltage regulator, which is a 32-tap transformer that can regulate the voltage ±0.1 pu and has a 2 V bandwidth. Each tap change increases the voltage by 0.0063 pu. The 2 V bandwidth on a 120 V base is equivalent to 0.0167 pu. This results in regularly having three valid power flow solutions, one for having the voltage regulator on each of the three taps in the bandwidth. An example is shown in Figure 93a where taps 1R, N, and 1L are all inside the voltage control band.

The number of possible solutions increases with a series of VREG's downstream of each other in succession on a long feeder. For example, if the upstream voltage regulator picks the tap near the top of the band, the downstream voltage regulator could have new possible solutions at lower tap positions.

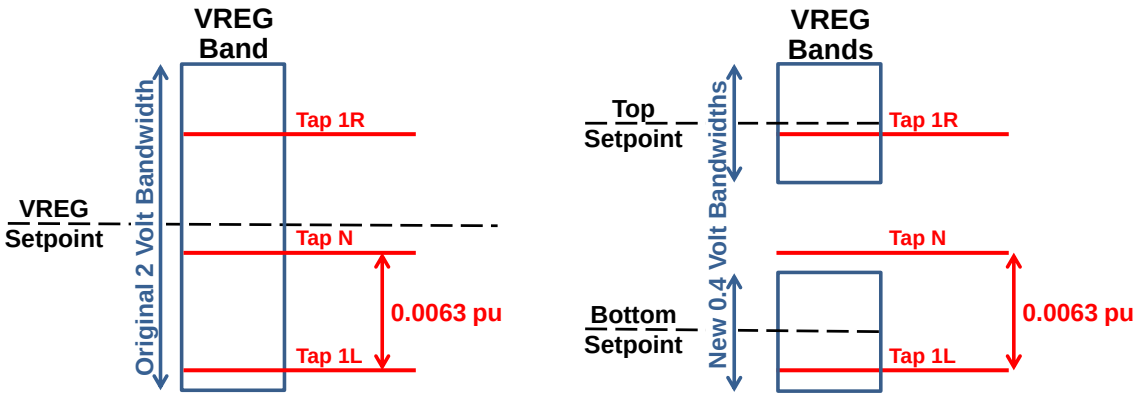


Figure 93. 32-tap VREG with 2 V bandwidth illustrating multiple possible solution states for tap position and the top/bottom of band solution algorithm.

Switching capacitors in voltage control mode also have a deadband, or hysteresis, in order to avoid constant switching. Capacitors are generally set to connect to a grid at a low voltage and disconnect from the grid at a high voltage. In between the on and off voltage thresholds, the capacitor could be in either the connected or disconnected state due to the hysteresis control. This is shown in Figure 94.

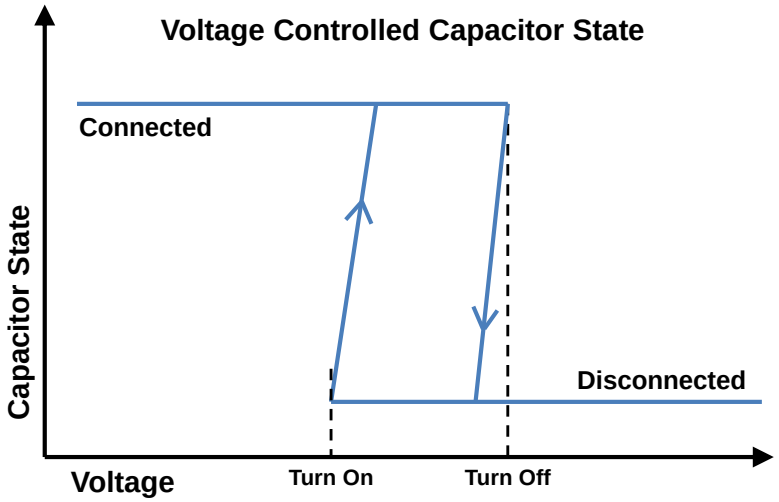


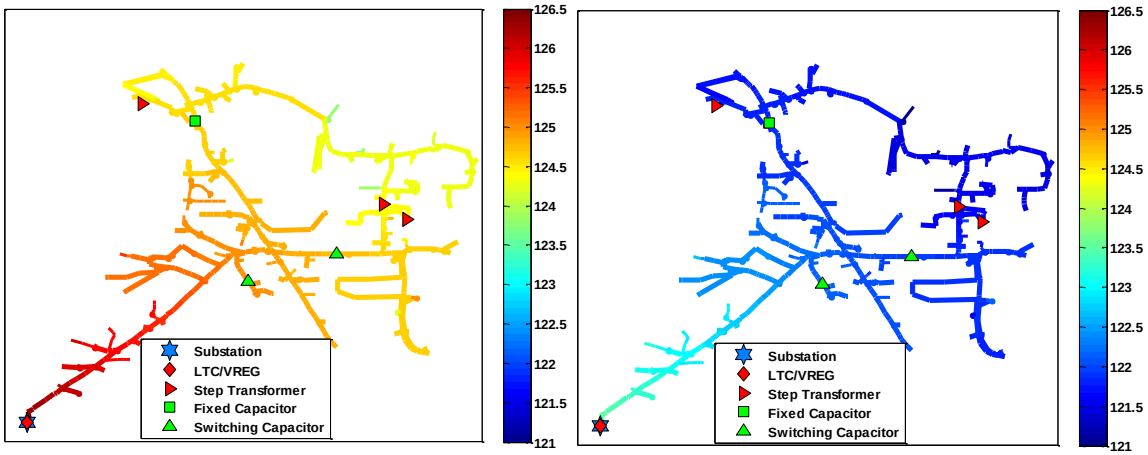
Figure 94. Capacitor state voltage hysteresis.

For distribution system simulations, generally the state of the capacitor and VREG tap can be found using external information. Historical SCADA data can include the state of the system for each time period, or analysis of SCADA data can be used to

detect switching events. When performing timeseries simulations, the particular tap at each instant is dependent on the previous state, so the tap is known from the historical load profile and the correct VREG control algorithm implemented in simulation. The possibility of several valid solutions on different taps creates an issue for the hosting capacity analysis methodology because the impact of PV to the distribution system is studied using steady-state snapshot simulations. There is no historical information, either SCADA or previous simulation timesteps, to know which tap each voltage regulation device should be on inside the allowed voltage bands. To prevent this uncertainty, we developed a method to investigate each scenario with all voltage regulation at both the top of band and the bottom of band separately. Each power flow solution and check for violations includes two independent power flow solutions at each side of the band to represent all valid power flow solutions. For voltage regulators, the tap is forced to the top of band or bottom of band by reducing the bandwidth of the control and changing the VREG setpoint for each top/bottom of band power flow solution. This is illustrated in Figure 93b. If the voltage control capacitors are within their hysteresis band, they are also checked for both the on and off state. The top of band solution represents the high voltage extremes, so the capacitors are connected if they are in the band. For bottom of band solutions, the capacitors in the hysteresis band are set to off. Every PV scenario is solved for both top and bottom of band control points.

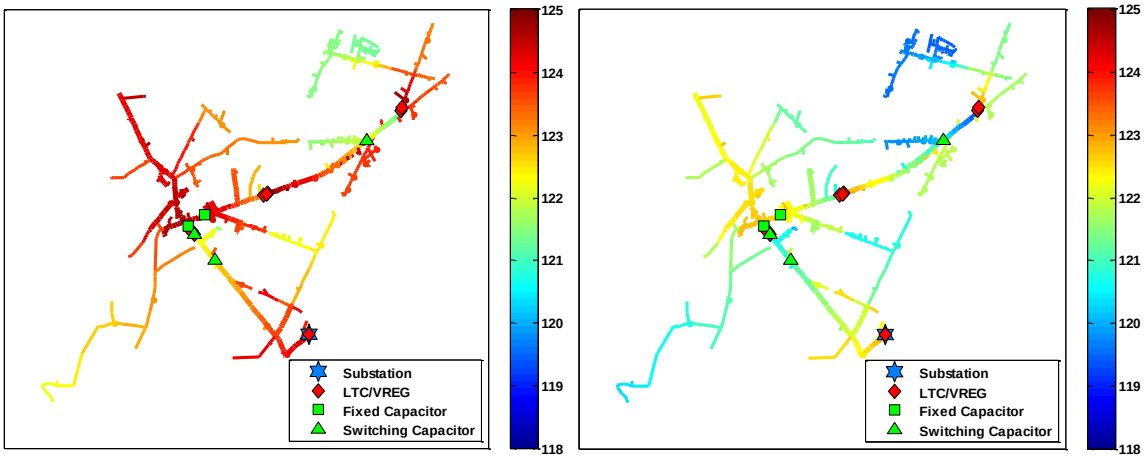
The differences in the feeder voltage profile depending on the top or bottom of band can be substantial. An example of the top and bottom of band voltages for feeder ML1 are shown in Figure 95. The substation LTC in ML1 has a set-point of 121.8V (LDC at R=6 V and X=2 V) with a 3.15V band on a 120V-base. Figure 95a shows ML1's LTC being forced to the top of the regulating band while Figure 95b shows it being forced to the bottom of the band. An example is also shown for J1 in Figure 96. J1's substation LTC and 3 voltage regulators all have a voltage set-point of 124V and a

bandwidth of 2V on a 120V-base. Figure 96a shows the circuit being forced to the top of the regulating band while Figure 96b shows it being forced to the bottom of the band.



(a) Top **(b) Bottom**

Figure 95. Circuit plots for ML1 contoured by bus voltage (120V-base) with the regulators set to a) the top of their bands and b) the bottom of their bands

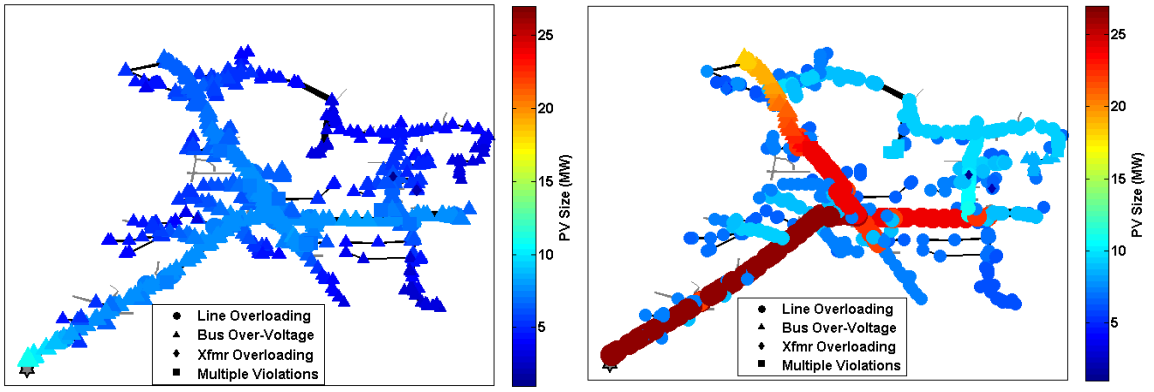


(a) Top **(b) Bottom**

Figure 96. Circuit plots for J1 contoured by bus voltage (120V-base) with the regulators set to a) the top of their bands and b) the bottom of their bands

With multiple possible taps inside the control band, the voltages in the system and hosting capacity of PV can be significantly impacted by which tap is selected in the power flow solutions. As example of the implications of voltage regulation being at the top or bottom of their bands, Figure 97a demonstrates the locational hosting capacity of

Murray Lake if all of the voltage regulation equipment is forced to the top-of-band while Figure 97b shows the locational hosting capacity if all of the voltage regulation equipment is forced to the bottom-of-band. In both simulations the voltage regulation equipment is locked on the specific tap at the top or bottom of band in the basecase and not allowed to change during the analysis. Over-voltage violations are considered for bus voltages outside ANSI Range A and thermal violations are considered at 100% of component rating. For the former, the average hosting capacity is 5.73 MW. For the latter, it is 11.51 MW. This shows a more than 100% increase in average hosting capacity for this feeder. Moreover, the top-of-band scenario has 94% of its buses' hosting capacities dictated by steady-state over voltages. Conversely, the bottom-of-band case has 90% of its buses' hosting capacities determined by line loading. Clearly, there is a profound effect of tap choice in hosting capacity evaluation. Therefore, it is imperative to account for it in such an analysis.



(a) Top **(b) Bottom**

Figure 97. ML1 at 70% load showing locational hosting capacity with voltage regulation locked at a) the basecase top-of-band and b) the basecase bottom-of-band

5.5 Temporary Over-Voltages (TOV) from PV Ramps

In order to accurately characterize extreme voltages that may occur on the feeder due to PV, it is necessary to simulate ramps in PV power to detect any potential

temporary over-voltage (TOV) conditions that may occur before the regulators react after their delay period. Solar irradiance can have very large variability and significant quick ramp rates. While, the size of the geographical footprint of the PV plant can smooth the expected variability compared to a point irradiance sensor [123], the power output can still ramp many MW's in a minute under extreme cases. For the distribution system, the short-term variability is significant because it can occur faster than the voltage regulation equipment can react. Most voltage regulation equipment has a delay of 30 to 90 seconds, so the 1-minute ramp ramps provide a reasonable comparison for the magnitude that PV can change before the distribution system has reacted. To analyze the impact of PV variability on the distribution system, the worst case scenarios with the highest ramp rates are studied. Looking at the top 0.1% of 1-minute ramps, a 32 MW plant can ramp more than 10.56 MW, and a 24.5 MW plant can ramp 8.58 MW [140]. Similarly, a 80 MW plant can ramp more than 14.4 MW in a minute [140]. From this, it is assumed that a large plant can ramp approximately 10 MW in the time delay of the distribution system.

For smaller plants, the per-unit ramp rates are higher, but the ramp in MW per minute is smaller. Small systems generally have 99.9% of their ramp rates under 50% of capacity. The worst ramp can be higher almost up to 70%, but almost all systems have a 1-minute ramp rate of 0.5 at 99.9%. This can be seen for a 5 MW system in [140], a 4.5 MW system in [140], 13.2 MW system in [141], and three systems greater than 10 MW in [142].

To simulate the impact of extreme PV power output ramps rates, a simple formula is used to calculate the ramp size. For smaller systems under 20 MW, a 50% ramp magnitude is studied. For larger systems greater than 20 MW, a 10 MW ramp magnitude is used in simulation. Both up ramps and down ramps are simulated for system impact. For the up ramp, the appropriate ramp magnitude is subtracted from the total PV size and OpenDSS is used to solve for the state of the voltage regulation equipment at the smaller PV output. The voltage regulation equipment is then locked and the PV output is

increased to full output. This is done for every PV deployment size and location. The down ramps are studied using a similar method of locking the voltage regulation equipment at full PV output and decreasing the PV size by the ramp magnitude.

The effect of PV ramping events is demonstrated on the voltage profile after up and down ramps. Feeder ML1 is shown in Figure 98 and J1 is shown in Figure 99. A 2.5MW PV plant was placed on both feeders, as shown by the star on each plot. Voltage regulation in each case is being forced to the top of their bands.

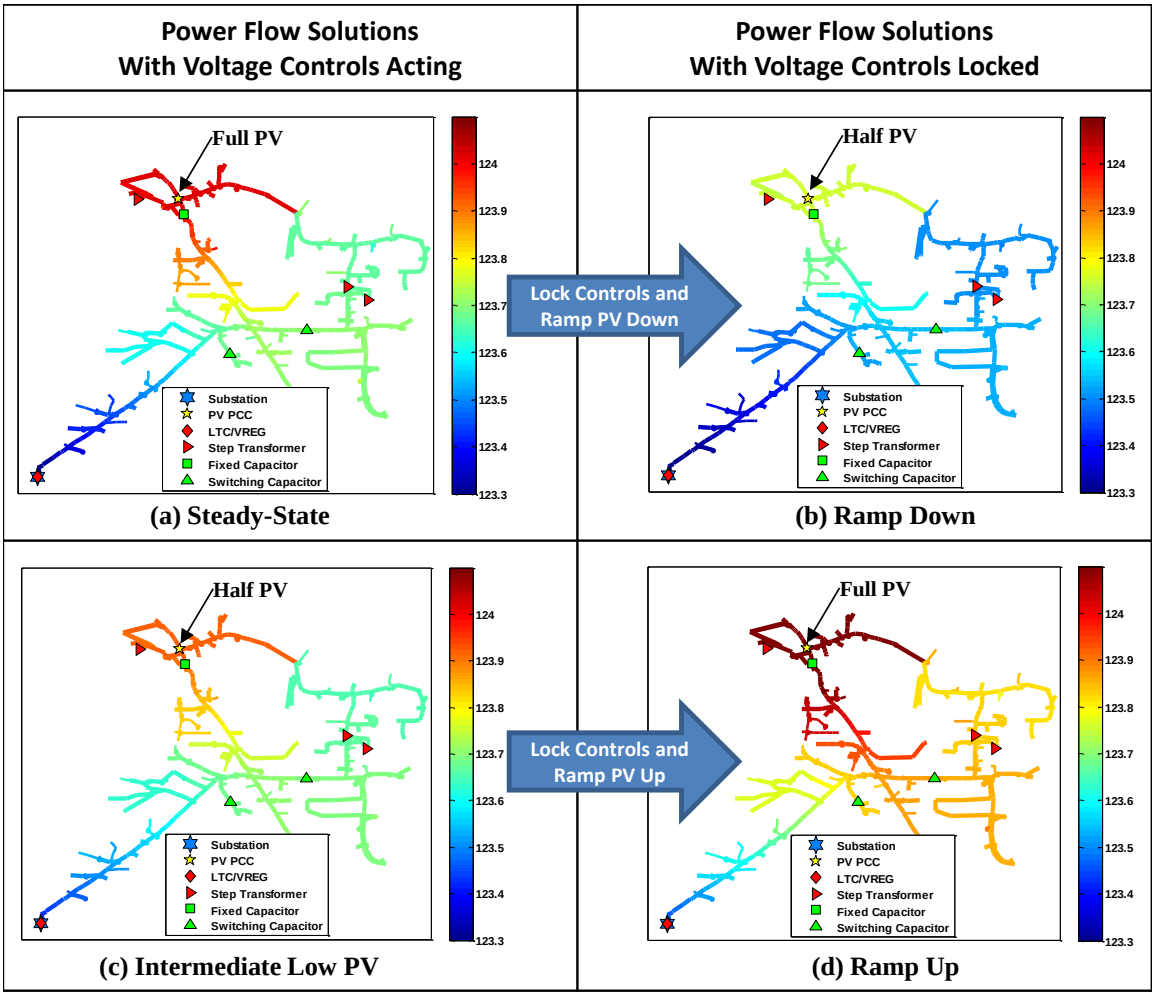


Figure 98. Circuit plots for Murray Lake at full load contoured by bus voltage (120V-base) with a 2.5MW PV system and voltage regulation at the top of their bands shown for the 4 different solve modes: a) Steady-state b) PV down ramp c) Steady-state before up ramp d) PV up ramp

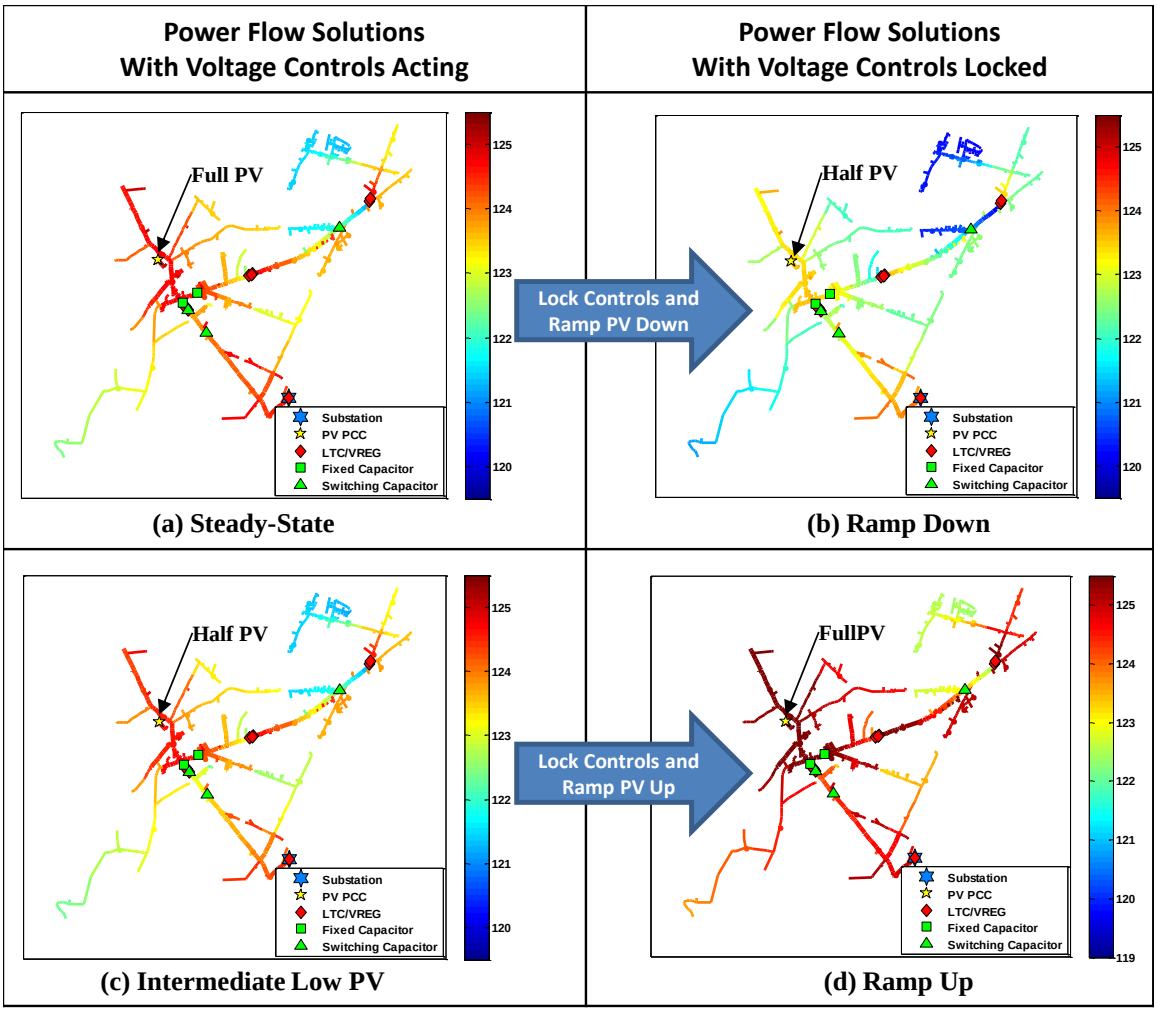


Figure 99. Circuit plots for J1 at full load contoured by bus voltage (120V-base) with a 2.5MW PV system and voltage regulation at the top of their bands shown for the 4 different solve modes: a) Steady-state b) PV down ramp c) PV steady-state before up ramp d) PV up ramp

Figure 98a and Figure 99a depict the results of a steady-state solve. For this solve mode, the PV is outputting rated power and the voltage regulation equipment is allowed to act freely, so as to settle into a steady-state solution at the top of the regulations bands. Once this steady-state solution is obtained and the pertinent data is recorded, the regulation equipment is locked. The PV system is then set to output half of its rated power (if the PV system's rated power is above 10MW, then it is set to output its rated power minus 10MW). After solving, we obtain the plots shown in Figure 98b and Figure 99b. The overall voltage profile of each feeder has decreased.

Now, with the PV system still outputting half its rated power, we once again allow the regulation equipment to act freely, obtaining a steady-state solution for the half-PV case. This solution is shown in Figure 98c and Figure 99c. This change allows the voltage profile to return to a state more similar to those shown in Figure 98a and Figure 99a. Lastly, to simulate an up ramp, the regulation equipment is now locked, and the PV system is set to output its rated power. The results of this are shown in Figure 98d and Figure 99d. As expected, this results in the most extreme high voltages in the figures.

While ramping events create more extreme voltages, they are also only temporary. For example, after 45 seconds, Figure 99d will return to Figure 99a as the regulators change taps. The temporary over-voltages (TOV) should not be compared to the ANSI C84.1 Range A standard (voltage must be less than 126 V) that applies to 10-minute average voltage in normal conditions. Since a ramp would be a temporary voltage violation and deviation of around 30 seconds until the voltage regulation equipment operates, ANSI C84.1 Range B (less than 127 V) can be used for these infrequent and limited periods where the corrective measures of the voltage regulation equipment bring the voltage back into Range A. Alternatively, the CBEMA/ITIC threshold (less than 132 V) for evaluating fluctuations could be used [146].

In the steady-state simulations without ramping events, all voltages in the system are compared to the ANSI C84.1 Range A standard [134]. All voltages in the simulations are also broken into the two service voltage categories using the 600 V threshold. For the steady-state simulations, the acceptable voltage range is 0.975-1.05 pu on the primary and 0.95-1.05 pu on the secondary.

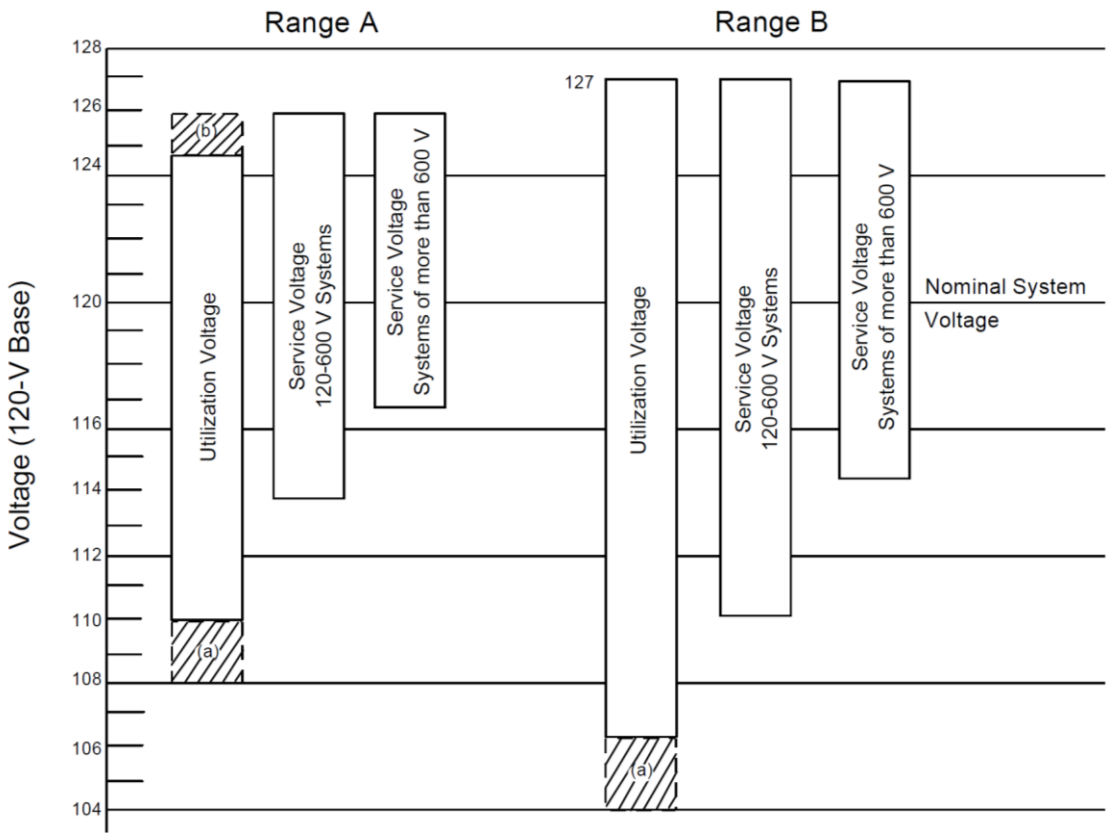


Figure 100. ANSI C84.1 Voltage Ranges

ANSI C84.1 Figure Notes:

a) The shaded portions of the ranges do not apply to circuits supplying lighting loads
b) The shaded portion of the range does not apply to 120 V - 600 V systems
c) The difference between minimum service and minimum utilization voltages is intended to allow for voltage drop in the customer's wiring system. This difference is greater for service at more than 600 volts to allow for additional voltage drop in transformations between service voltage and utilization equipment.

As an example, the locational hosting capacity is calculated for each bus in J1 using the ANSI C84.1 Range B threshold for determining over-voltage violations during PV ramping events. Figure 101 shows a pie chart of what type of violation limited the locational hosting capacity for all buses in J1 at peak load. When considering steady-state (SS) scenarios along with the up and down ramps, 49% of the violations for J1 at peak load are cause by over-voltages during a PV up-ramp. When neglecting these scenarios

and only considering steady-state violations, the hosting capacity at those buses is 763 kW higher on average.

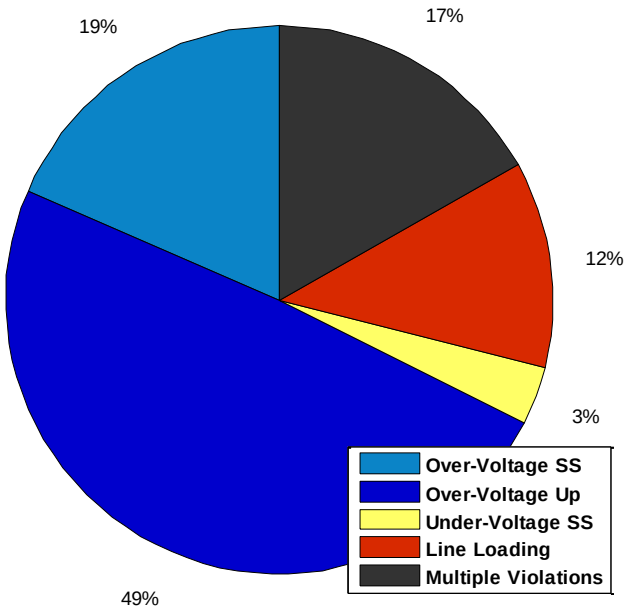


Figure 101. Pie chart of violation causes for J1 at peak load when considering ramp and steady-state violations

5.6 Analysis Methodology

The flow chart in Figure 102 shows the entire hosting capacity methodology for analyzing each bus location by increasing the PV size until 10 MW or until there is a violation. The four power flow solutions are shown for steady state of PV output, a down ramp, and an up ramp in PV output. The loop for trying the possible extreme ends of the power flow solutions inside the band of each voltage regulator device is shown when the VREG's and capacitors are set to bottom of band and then top of band.

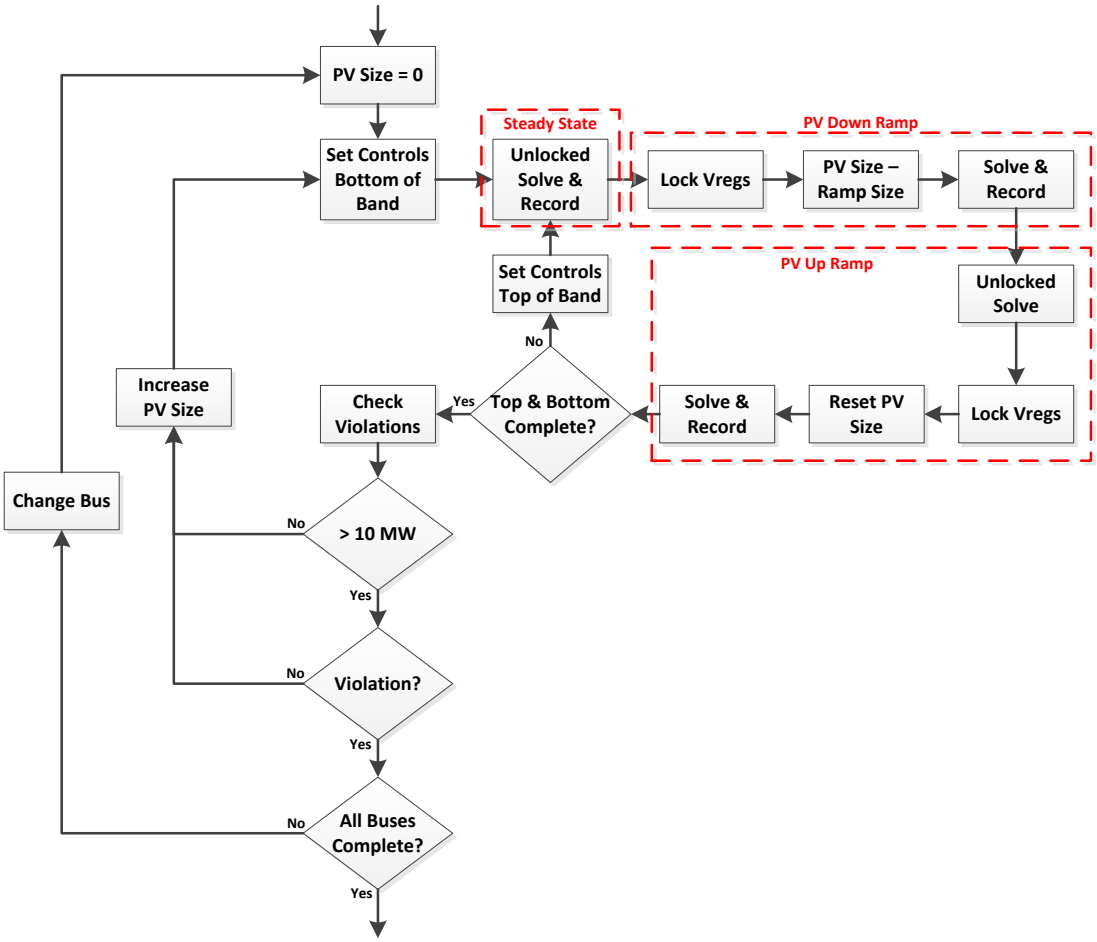


Figure 102. Flow chart of solution methodology for hosting capacity for single large PV plants.

For some feeders at certain load levels, violations exist on the feeder before PV is even added. This could cause the simulations to end immediately and the hosting capacity to be listed as zero PV that can be added to the feeder, due to the pre-existing violation. In some cases, the violation is an under-voltage, and PV actually improves the voltage, alleviating the violation at higher penetration levels. Situations like this should not classify the PV hosting capacity as zero, even though there is a violation. In other words, if the utility has allowed specific voltages or line loading on the feeder (even if it is slightly overloaded or outside standards), PV interconnections should be allowed as long as they improve the state of the feeder.

For each violations analysis, the basecase values are stored for each load level. For example, the voltage at each bus will be compared to the voltage at that bus in the basecase. If the increase in PV system size is alleviating the violation (decreasing a maximum voltage / increasing a minimum voltage), the analysis does not consider this a violation caused by PV, even though the values are outside the standards. The same methodology is applied for the thermal loading of each line and transformer. The simulation proceeds to increase the PV system size until the hosting capacity is reached when values are outside standards and any values being checked for violations are worse than the basecase.

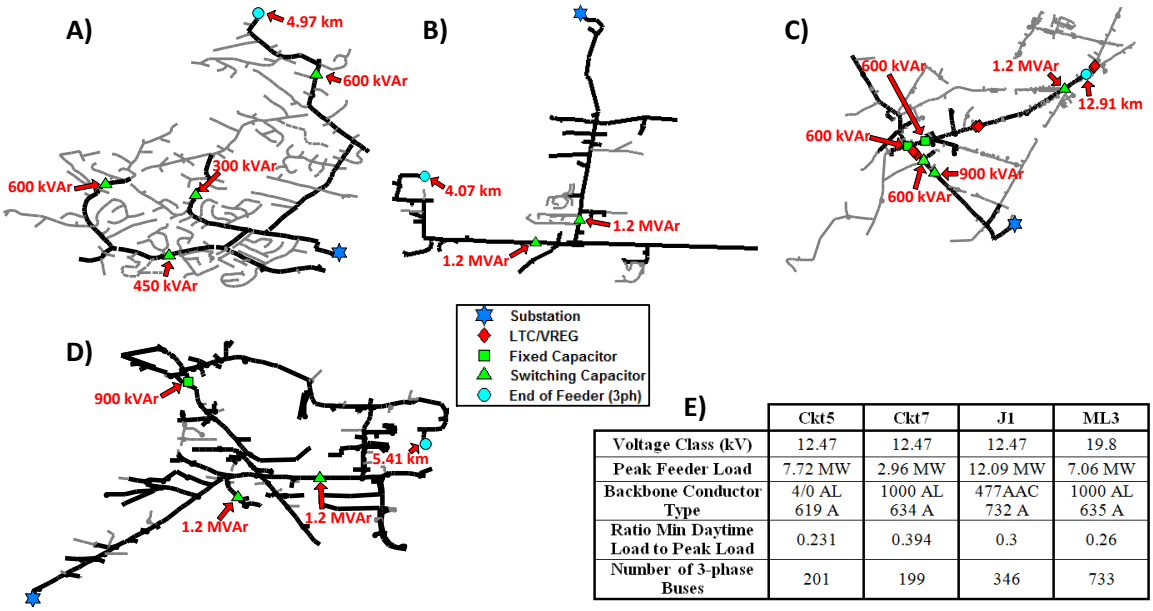
5.7 Determining Feeder PV Impact Signatures

In order to improve the interconnection study process, the use of feeder PV impact signatures are proposed to group feeders by allowable PV size as well as by their limiting factors for the interconnection. The feeder signature separates feeders into different impact regions with varying levels of PV interconnection risk, accounting for impact mitigation strategies and associated costs. This locational information improves the speed and accuracy of the interconnection screening process. The interconnection risk analysis methodology is based on the feeder and interconnection parameters such as: feeder type, feeder characteristics, and location and size of PV. PV impact signatures are calculated and demonstrated for four distribution systems.

The work in this section contributes to the overall objectives of developing a Feeder Impact Risk Score Technique (FIRST), which seeks to quantify the risk level of interconnection requests by comparing and matching feeders to clusters of known prototypical feeder topologies and characteristics. The category of feeders will display similar interconnection risks, limiting factors, interconnection zones, and optimal mitigation strategies, thus improving the speed and accuracy of the interconnection screening process. By performing thorough PV interconnection simulations on several

feeders, the most critical characteristics that cause adverse impacts can be collected and analyzed for general feeder behavior and universal applicability.

The analysis is demonstrated for four distribution feeders. These feeders represent a range of possible topologies and characteristics, which result in very different feeder impact signatures. The topology and locations of major circuit elements are shown in Figure 103A through Figure 103D, and relevant feeder details are listed in the table in Figure 103E. The four feeders being used are referred to as Ckt5, Ckt7, J1, and ML1. Ckt5 and Ckt7 are publically available as example feeders in OpenDSS [117].



E)

	Ckt5	Ckt7	J1	ML3
Voltage Class (kV)	12.47	12.47	12.47	19.8
Peak Feeder Load	7.72 MW	2.96 MW	12.09 MW	7.06 MW
Backbone Conductor Type	4/0 AL 619 A	1000 AL 634 A	477AAC 732 A	1000 AL 635 A
Ratio Min Daytime Load to Peak Load	0.231	0.394	0.3	0.26
Number of 3-phase Buses	201	199	346	733

Figure 103. Information for four example distribution feeders: A) Ckt5 topology, B) Ckt7 topology, C) J1 topology, D) ML3 topology, and E) feeder characteristics.

The hosting capacity analysis methodology presented in the previous sections is used to iterate through possible interconnection locations, sweeping through a range of PV sizes up to 10MW at each location. The number of potential interconnection locations on 3-phase buses varies between feeders, shown in the table in Figure 103E. The total number of scenarios considered is a function of the total number of PCC locations multiplied by the total number of PV system sizes.

For each scenario, the algorithm solves the power flow and checks for any violations on the feeder [136]. For each scenario (i.e. each specific PV size and PCC combination) both the maximum and minimum daytime load are simulated, where daytime is defined as being between 10am and 2pm [63]. Any feeder violations that were observed at either of those load levels are flagged for the scenario at which it occurred. Steady-state and the extreme PV up and down ramps described in the previous section are simulated, along with the separate simulations for all voltage regulation equipment forced to the top and bottom of its band.

After iterating through all of the scenarios, the data and violations of each scenario are stored. The extensive analysis results allow for thorough feeder impact assessments. Details of the problematic scenarios give insight to the most important feeder and PV characteristics that result in violations. This allows for a more technically customized approach than current screening methods.

After performing the analysis of hundreds of thousands of PV scenarios for each of the four feeders, the results can begin to be classified by how often a given PV size is permissible at different locations around the feeder. The figures below (Figure 105 - Figure 108) classify the violations into regions based on either voltage or thermal violations. The definition for each region is shown in Figure 104. Region A and Region B both contain allowed interconnection locations that have no violations. Region A is the area that would be found using a total feeder hosting capacity approach that would give one number for the maximum allowed PV anywhere on the feeder. The feeder hosting capacities, i.e. the boundary between Region A and Region B, are shown for each feeder in Table 15. Region A includes the PV sizes below which a system could be interconnected anywhere on the feeder without further investigation. The other regions refer to system sizes that require further consideration before determining the feasibility of a PV system. Region B contains interconnections that are ultimately allowed but must use some locational details such as PCC distance to the substation and/or conductor type

before making this assessment. Regions C, D, and E all include interconnections that have at least one violation and therefore cannot be connected given the current state of the feeder without some mitigation. Regions C, D, and E contain interconnections that respectively result in either only voltage violations, only thermal violations, or both voltage and thermal violations.

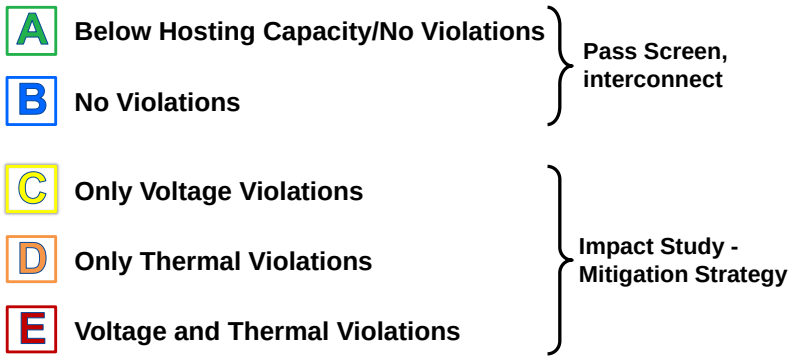


Figure 104. Feeder regions legend.

The feeder signatures (Figure 105 – Figure 108) show the differences between the feeders in the defining factors for their areas of risk. The best way to analyze the figures is to look at individual vertical slices in the graph. For example, for the vertical profile of a 5 MW PV interconnection on Ckt7, 11% of the possible interconnection buses are in Region E, 55% are in Region D, and 34% are in Region B. Ckt7 is almost entirely defined by line thermal limits, which makes this 3.5MW threshold a costly barrier to surpass. Ckt5's hosting capacity, on the other hand, is completely defined by over-voltage violations. The barrier present around 1.6 MW is easily increased to 3.5+ MW by altering LTC setpoints. Feeder ML1, in contrast to the other two, is a combination of only voltage limits and only line thermal limits.

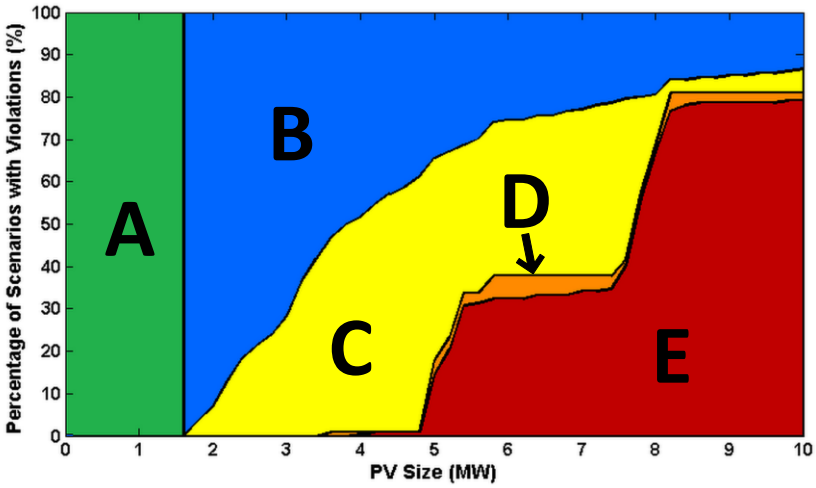


Figure 105. Ckt 5 feeder signature regions.

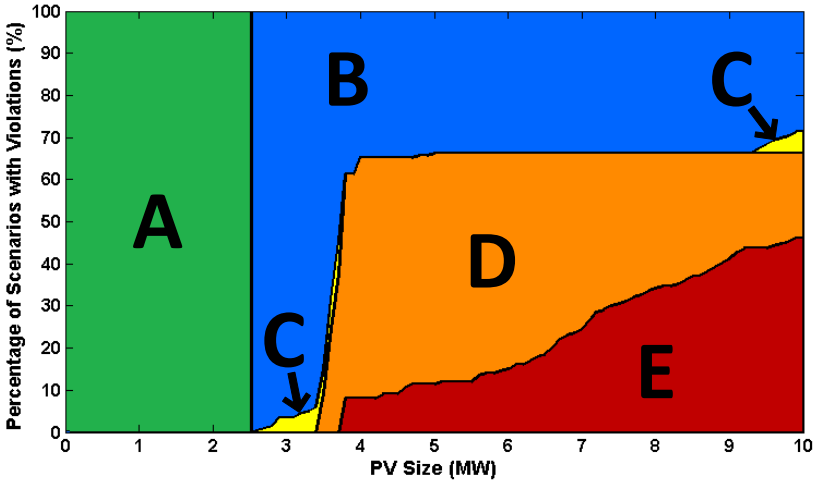


Figure 106. Ckt7 feeder signature regions.

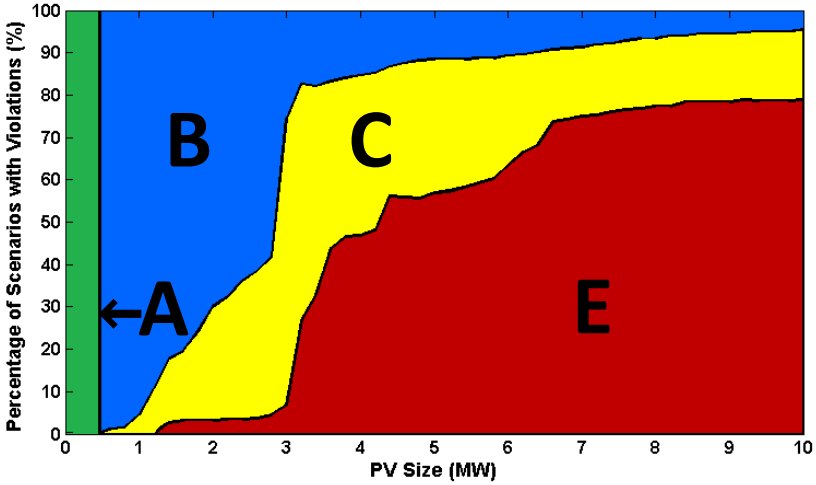


Figure 107. J1 feeder signature regions.

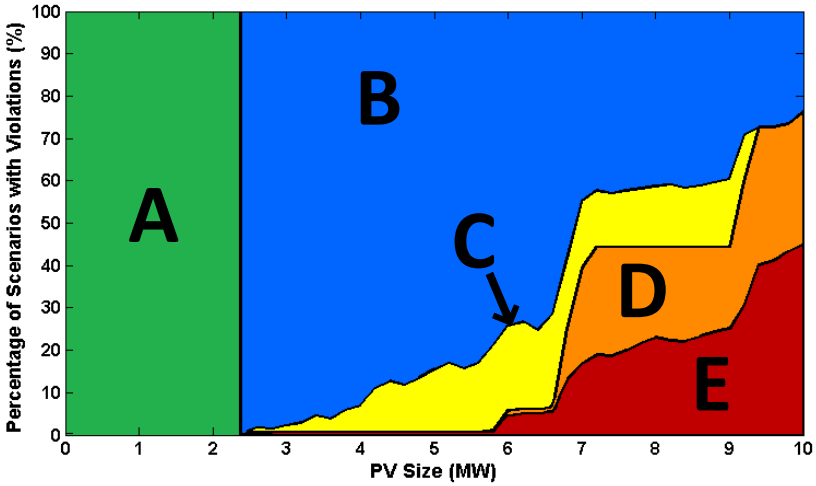


Figure 108. ML1 feeder signature regions.

Looking at Table 15, there is significant possible improvement in the 15% of peak load interconnection screen [63]. For example, the 15% screen would allow quite a few PV scenarios up to 1.8 MW on J1 that would cause issues on the distribution system. In fact, 8% of the cases allowed by the 15% screen for J1 are false-positives. The other argument is the number of PV scenarios that would not cause any violations that the 15% screen does not allow. On average for the four feeders, there are 6.4 times more allowed PV scenarios (Region A + Region B) than are allowed by the 15% screen.

Table 15. Percent of PV Interconnection Scenarios in Each Region.

	Ckt5	Ckt7	J1	ML1
15% Screen	1.1 MW	0.5 MW	1.8 MW	1.0 MW
Hosting Capacity	1.6 MW	2.5 MW	0.4 MW	2.4 MW
Region A	16.0 %	25.0 %	4.0 %	24.0 %
Region B	31.6 %	32.0 %	26.1 %	49.5 %
Region C	23.7 %	0.7 %	23.3 %	8.4 %
Region D	1.7 %	26.5 %	0.1 %	8.5 %
Region E	27.0 %	15.8 %	46.5 %	9.6 %

The simulation results presented show how a PV hosting capacity analysis can be used to obtain a feeder impact signature. This feeder signature separates a feeder into different impact regions that present varying amounts of PV interconnection risk. The

regions relate to specific zones of the feeder where PV: is easily interconnected, possibly requires some impact mitigation strategies, or definitely presents risks that may be cost-prohibitive. Incorporation of locational information improves the speed and accuracy of the interconnection screening process by providing a more technically-based determination of the PV limits of a feeder. This analysis is expanded to a larger set of feeder topologies and PV interconnection types in later sections.

5.8 Feeder PV Impact Zones

The purpose of performing the large number of PV scenario simulations is to begin analyzing patterns of feeder characteristics that can be translated into levels of feeder risk for PV interconnection impacts. As seen in the previous section, there is significant advantage to including interconnection locational information in the screening criteria to allow for interconnections without violations in Region B that are greater than the hosting capacity. In each of the examples, Region B contained the greatest number of cases, indicating that this could be a very beneficial realm to exploit. Simple parameters such as distance to the substation and conductor type can allow a distribution feeder to be classified into interconnection zones. For example, the hosting capacity of Ckt5 is 1.6 MW, but the locational hosting capacity of specific points on the feeder is much higher. In Figure 109, the feeder interconnection zone map for a 6 MW interconnection on Ckt5 shows that there are 25% of the buses that are capable of handling such a system. The feeder zone maps also improve interconnection screening through showing the risk associated with the interconnection. At 6 MW, half the buses with interconnection issues are only caused by voltage violations that may be easily fixed by changing voltage regulation equipment settings or adjusting the power factor on the PV inverter.

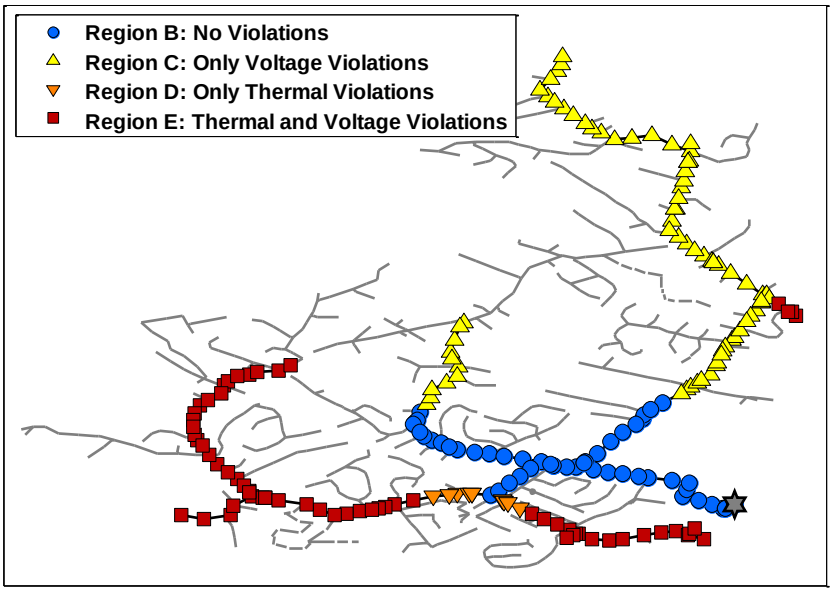


Figure 109. Feeder interconnection zone map of 3-phase line sections for a 6 MW PV plant on Ckt5.

5.9 Analysis of 50 Distribution Feeders

The PV hosting capacity work presented in the previous sections was developed to analyze the risk associated with different feeder topologies and characteristics. The analysis is performed for a large range of different distribution systems under high PV deployment scenarios. In total, 50 different feeders are simulated so that the risks associated with interconnecting PV on different feeder topologies can be determined. This novel and very detailed analysis has never been performed on so many feeders before. Previous work includes hosting capacity analysis of 18 feeders [86], and 28 feeders [155]. The 50 feeders analyzed will provide new insight into the feeder characteristics and locational information that correlates with high penetrations of distributed PV being able to be installed. First, the database of 50 feeders is described, along with an overview of the characteristics of these feeders. Second, the hosting capacity analysis results are presented for the feeders.

5.9.1 Feeder Characteristics

Each of the 50 feeders is an actual distribution systems located around the United States. For proprietary information reasons, the locations of each feeder cannot be disclosed, and all names have been removed. The models were provided by approximately 10 different utilities, encompassing everything from the west coast to the east coast. For all except 3 feeders, the utility also provided at least a year of substation SCADA measurements for the feeder. There is also a nice range of feeders, including industrial, urban, commercial, rural, and agricultural. Each model includes the full details about substation impedance, voltage regulator settings, and capacitor switching controls. The load allocation method used for each feeder varies depending on the data provided, such as billing kWh data, metered peak demand, etc. In each case, the feeder peak load measurement was used as the load allocation time. Each feeder also includes an approximate model of the secondary system, often using standard transformer impedances by kVA size and 100 feet of 1/0 triplex cable between the transformer and the customer. Due to the number of feeders, some infrequent features are captured, such as 3-wire feeders without neutral wires and feeders with multiple voltage levels due to step-down transformers.

The voltage classes of the feeders range from 4 kV to 34.5 kV. Figure 110 shows the number of feeders at each voltage class. As expected, approximately two-thirds of the feeders are at the 12/12.47 kV voltage class. There is also a range in the incoming transmission system voltage at the substation for each feeder. The high-voltage transmission side ranges from 46 kV to 230 kV.

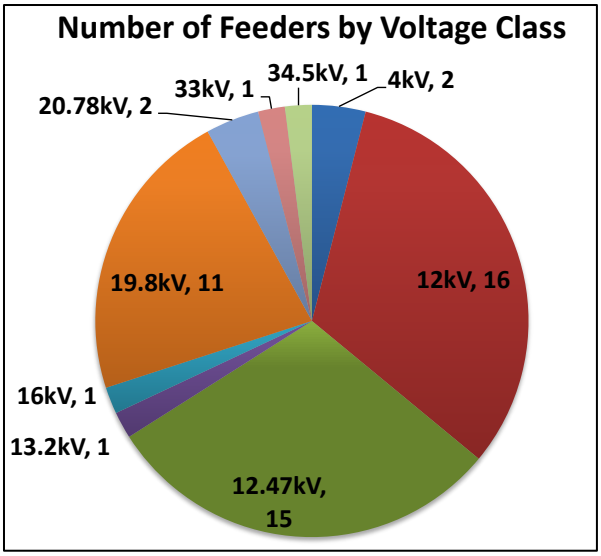


Figure 110. Pie chart of the voltage class of the 50 feeders.

The majority of the feeders (41 of 50) have no voltage regulators on the feeder itself, but as seen in Figure 111, there can be up to 6 regulators per feeder. In total, there are 25 voltage regulators in the database of 50 feeders. There are several different types of voltage regulators, including wye-connected phase regulators, gang-operated delta-connected regulators, and open-delta regulators. Two of the feeders also include boosters that increase the downstream voltage using a fixed tap.

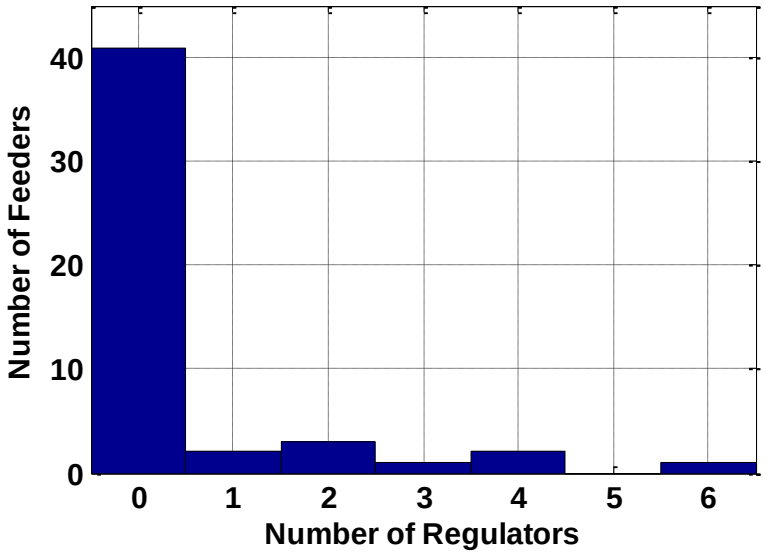


Figure 111. Histogram of the number of voltage regulators on each of the 50 feeders.

Both the fixed and switching capacitors are modeled for each feeder. As seen in Figure 112, the feeders have between 0 to 7 capacitors per feeder. The feeder with 7 capacitors has a total of 9.9 MVAR of capacitance on the feeder. Most of the switching capacitors are voltage-controlled, but there are also time-controlled, temperature-controlled, kVAR-controlled, time-biased voltage-controlled, and seasonally-controlled capacitors.

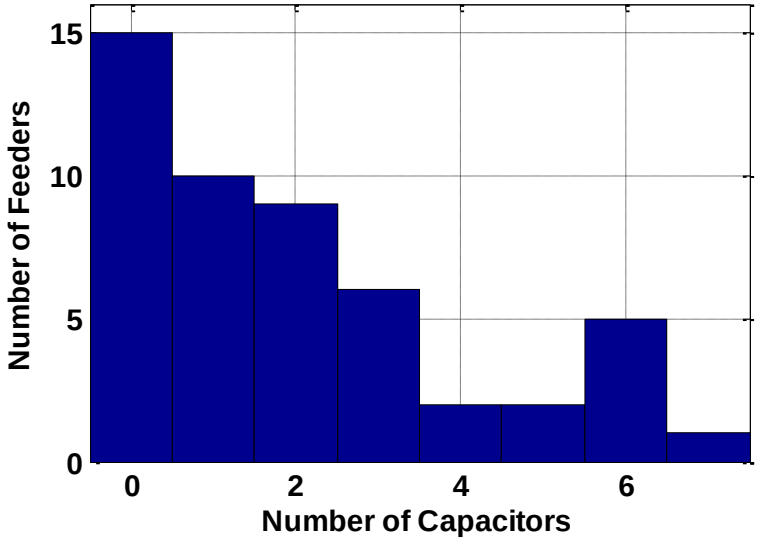


Figure 112. Histogram of the number of capacitors on each of the 50 feeders.

Figure 113 shows the range in the peak load for each of the feeders. The lowest feeder only has a peak of 0.6 MW, and the highest is 28.5 MW. Of course the feeder peak load is highly correlated with the voltage class of the feeder. For the hosting capacity analysis, the minimum and maximum load measured during the period of 10am to 2pm for the year is used. As a percentage of the peak load, the minimum daytime load ranges from 12% to 75% of peak load. The maximum daytime load ranges from 71% to 100% of peak load depending on the feeder.

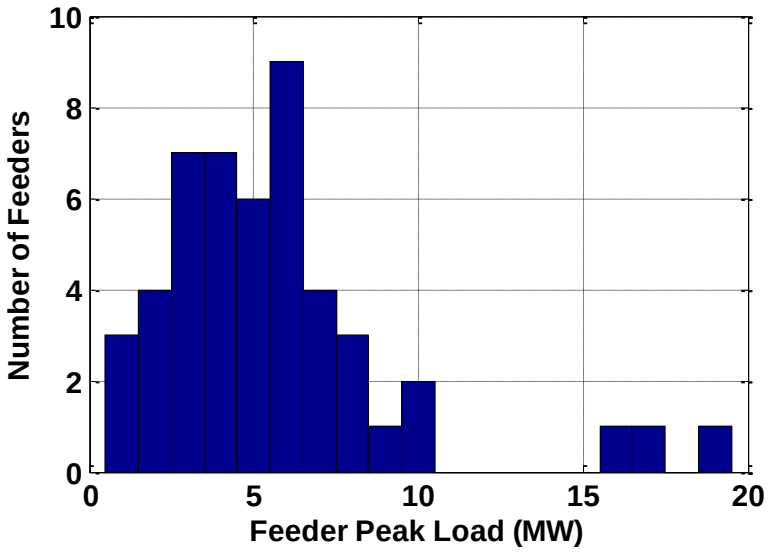


Figure 113. Histogram of the peak load (MW) for each of the 50 feeders.

The 50 feeders range in length from 1.8 km to 29.4 km. Figure 114 shows the total length of 3-phase and 1&2-phase medium-voltage (MV) conductor vs. the farthest 3-phase bus for each feeder. There is a significant spread in the length and amount of conductor for each feeder. The ratio of 3-phase conductor to non-3-phase conductor also varies significantly between feeders.

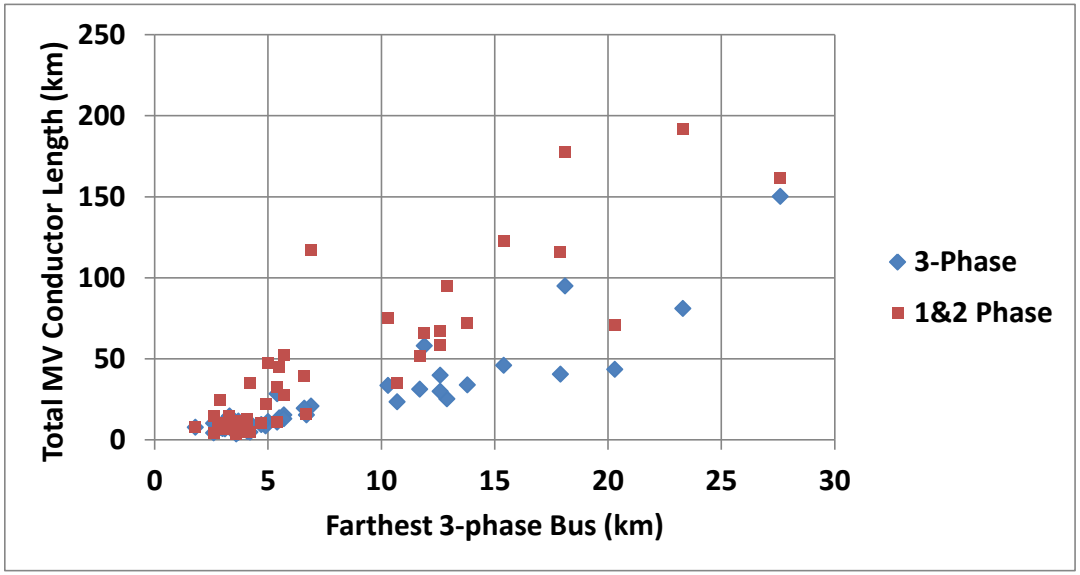


Figure 114. Total 3-phase and 1&2-phase medium-voltage (MV) conductor vs. the farthest 3-phase bus for each feeder.

Similar to the length of feeder, the number of buses in each feeder model varies significantly from 125 to 6001 buses per feeder. Many of the key characteristics are shown for each of the 50 feeders in Table 16 and Table 17. For the hosting capacity analysis, only 3-phase buses that are at least 20 meters away from the substation and at the voltage class of the feeder are tested. The number of PV test buses for each feeder is shown ranging from 69 to 1275 buses. The ampacity ratings of the 3-phase medium-voltage (MV) conductors is shown for each feeder in the tables. The feeder backbone is defined as the 3-phase MV line with the highest ampacity rating that has at least 500 meters of conductor in the feeder.

Table 16. Characteristics of Feeders 1 – 25.

Name		Load			Conductor Length (km)			3-Phase MV		Regulation		Capacitors			Buses	
	Voltage (kV)	Feeder Peak (MW)	Daytime Peak (MW)	Daytime Min (MW)	Farthest 3-phase Bus	Total MV 3phase	Total MV 1&2 Phase	Back-bone	Lowest	VREGs	Boosters	Total Cap kVAr	Fixed Caps	Switch Caps	Total Buses	PV Test Buses
Ckt5	12.47	7.35	6.74 (91%)	1.74 (23%)	5	11.2	36.4	619	163	0	0	1950	0	4	2998	201
Ckt7	12.47	5.67	5.48 (96%)	2.27 (39%)	4.1	9.1	3.8	637	160	0	0	2400	0	2	1246	199
Ckt24	34.5	28.45	28.45 (100%)	6.06 (21%)	6.9	20.9	96.2	650	195	0	0	3300	3	0	6001	351
ML1	19.8	6.93	6.93 (100%)	2.52 (36%)	5.4	28.5	3.9	635	190	0	0	3300	1	2	1266	727
J1	12.47	6.34	5.73 (90%)	1.04 (16%)	12.9	25.3	69.4	732	142	3	0	3900	2	3	3433	346
K1	13.2	4.86	4.63 (95%)	1.38 (28%)	5.5	13.5	31.1	900	155	0	0	300	1	0	1282	203
M1	12.47	5.82	5.53 (95%)	1.65 (28%)	2.9	7.8	16.9	400	400	0	0	3600	0	3	2596	260
QB1	4	2.21	1.88 (85%)	0.63 (28%)	2.8	6.6	2.1	582	110	0	0	0	0	0	1489	121
QL1	20.78	18.63	16.91 (91%)	4.96 (27%)	12.6	30	37.3	745	100	0	0	9900	1	6	5259	547
QL2	12	5.16	5.07 (98%)	1.37 (26%)	2.6	10.2	4.6	338	105	0	0	2400	1	1	2319	224
QM1	12	6.1	5.87 (96%)	1.92 (29%)	23.3	81	110.7	745	100	4	1	3900	1	5	5189	767
QN1	20.78	16.71	16.08 (96%)	6.23 (37%)	10.3	33.5	41.3	838	110	0	0	9600	0	6	4646	583
QS1	12	9.23	8.90 (97%)	1.95 (19%)	11.9	58.1	7.5	515	100	2	0	6000	0	6	2170	473
QW1	12	8.44	8.29 (98%)	1.13 (13%)	27.6	150.1	11.4	745	100	4	1	3900	2	4	2438	861
UQ11	12.47	3.36	3.13 (93%)	0.95 (28%)	4.9	8.6	13.5	574	100	0	0	600	1	0	732	122
UQ12	12.47	6.06	5.31 (87%)	1.63 (27%)	5.7	15.4	37.1	574	100	0	0	1800	4	0	1538	164
UD11	12.47	1.64	1.57 (96%)	0.66 (40%)	5.7	13.1	14.5	340	100	0	0	600	2	0	766	148
UD12	12.47	0.59	0.54 (92%)	0.23 (34%)	15.4	45.9	76.4	340	100	0	0	900	2	0	2394	425
UD13	12.47	1.12	1.10 (98%)	0.45 (39%)	20.3	43.5	27.3	540	100	2	0	300	0	1	784	152
UD14	12.47	0.86	0.85 (100%)	0.25 (27%)	10.7	23.4	11.8	340	100	0	0	300	1	0	675	157
UT11	12.47	6.89	5.95 (86%)	2.42 (34%)	12.6	39.9	18.5	574	100	0	0	1200	3	0	581	248
UT13	12.47	5.04	4.35 (86%)	1.77 (34%)	6.7	15.4	0.8	540	100	0	0	600	1	0	416	180
UT16	12.47	3.9	3.49 (89%)	1.44 (36%)	4.7	9.5	1.1	574	100	0	0	0	0	0	215	91
UT18	12.47	4.04	3.62 (89%)	1.51 (36%)	5.4	10.9	0.2	574	100	0	0	600	2	0	343	138
UT19	12.47	2.63	2.63 (100%)	0.80 (30%)	3.4	9.1	0.5	574	100	0	0	0	0	0	168	69

Table 17. Characteristics of Feeders 26 – 50.

Name		Load			Conductor Length (km)			3-Phase MV		Regulation		Capacitors			Buses	
	Voltage (kV)	Feeder Peak (MW)	Daytime Peak (MW)	Daytime Min (MW)	Farthest 3-phase Bus	Total MV 3phase	Total MV 1&2 Phase	Back-bone	Lowest	VREGs	Boosters	Total Cap kVAr	Fixed Caps	Switch Caps	Total Buses	PV Test Buses
DA1	12	4.43	4.37 (99%)	0.72 (16%)	4.2	10.3	24.5	770	108	0	0	2400	0	2	2376	165
DA2	12	10.35	8.93 (87%)	1.64 (16%)	18.1	95	82.6	770	108	6	0	3600	2	1	5839	1275
DC1	12	8.08	6.14 (76%)	3.70 (46%)	6.6	19.5	20.1	1060	108	0	0	2400	2	0	5056	446
DC2	12	3.6	2.55 (71%)	0.62 (17%)	17.9	40.5	75.1	770	108	1	0	1200	0	1	3411	548
DE1	12	7.85	7.85 (100%)	1.74 (22%)	3	6.9	0.2	770	130	0	0	1200	1	0	560	336
DK1	12	3.59	3.59 (100%)	0.74 (20%)	1.8	7.7	0.2	580	115	0	0	0	0	0	873	500
DS1	12	10.2	8.13 (80%)	1.49 (15%)	13.8	33.9	38	770	130	2	0	1200	0	1	5504	822
DV1	12	3.42	3.39 (99%)	0.42 (12%)	11.7	31.3	20.2	770	50	0	0	1200	0	1	1505	424
GL1	19.8	3.27	3.19 (97%)	2.05 (61%)	3.7	5.7	0	380	150	0	0	0	0	0	206	133
GL2	19.8	2.23	2.21 (99%)	1.28 (56%)	4.2	4.8	0	380	150	0	0	0	0	0	186	119
GL3	19.8	2.61	2.39 (91%)	1.08 (40%)	3.6	3.6	0	380	230	0	0	0	0	0	125	73
GL4	19.8	2.51	2.38 (95%)	1.62 (63%)	2.6	4.3	0	380	175	0	0	0	0	0	152	92
GL5	19.8	3.97	3.86 (97%)	1.91 (47%)	3.7	4.6	0	475	115	0	0	0	0	0	193	119
GL6	19.8	4.75	4.67 (98%)	1.35 (28%)	4.1	5.1	0	380	175	0	0	0	0	0	208	122
GN1	19.8	2.86	2.85 (100%)	2.16 (75%)	3	10.1	0	380	230	0	0	0	0	0	131	84
GN3	19.8	5.55	5.53 (100%)	4.23 (75%)	3.7	11.5	0	380	230	0	0	0	0	0	156	101
GN5	19.8	5.06	5.05 (100%)	3.61 (70%)	3.3	14.7	0	380	175	0	0	0	0	0	197	135
GN7	19.8	7.4	7.21 (97%)	1.03 (14%)	3.1	6.8	0	545	230	0	0	0	0	0	129	82
CD1	4	1.84	1.62 (88%)	0.33 (18%)	3.3	4.7	3.5	559	128	0	0	600	0	2	533	69
CG1	12	6.35	6.29 (99%)	0.85 (13%)	15.5	60.8	2.1	605	112	0	0	4800	0	6	1366	496
CH1	33	16.48	15.84 (96%)	5.11 (31%)	29.4	42.7	0	920	160	0	0	0	0	0	142	134
CL1	16	5.87	5.21 (89%)	1.97 (33%)	4.2	13	1.9	605	112	0	0	3000	0	3	1096	319
CO1	12	6.41	5.80 (91%)	1.52 (24%)	21.4	35.9	30.4	920	112	1	0	2700	1	4	2970	501
CS1	12	5	4.92 (98%)	1.95 (39%)	4.7	12.2	7.4	559	112	0	0	1200	0	1	1226	273
CV1	12	4.29	4.00 (93%)	1.13 (26%)	6.6	10.3	4.1	605	112	0	0	1500	1	1	484	153

5.9.2 Feeder Results

The impact of PV on distribution system operations is highly dependent on the voltage level of the feeder. At higher voltage levels, the same size PV system will inject less current at the feeder voltage. For this reason, the hosting capacity analysis has been split into four different voltage categories. The first category is 4 kV feeders that are only analyzed up a maximum size of 5 MW of PV. The second category of 12-14 kV feeders are analyzed up to 10 MW. The third category of 16-21 kV feeders are analyzed up to 15 MW. The fourth category of 33-35 kV feeders are analyzed up to 20 MW.

The detailed results for each feeder are included in Appendix B. As an example and to describe each figure, feeder QS1 is shown here.

First, the circuit diagram topology is shown in Figure 115 with the key components marked. The capacitor marker shows if the capacitor is fixed or switching, and the arrow text gives the size of each capacitor. For QS1, the capacitors are seasonally switching, so for the analysis they are fixed into the correct state depending on the time of year. In Appendix B, below the feeder diagrams, the voltage level of the feeder and feeder load are shown. For QS1, the peak load is 9.25 MW, and the maximum and minimum daytime load (10am to 2pm) is 8.92 MW and 1.96 MW respectively.

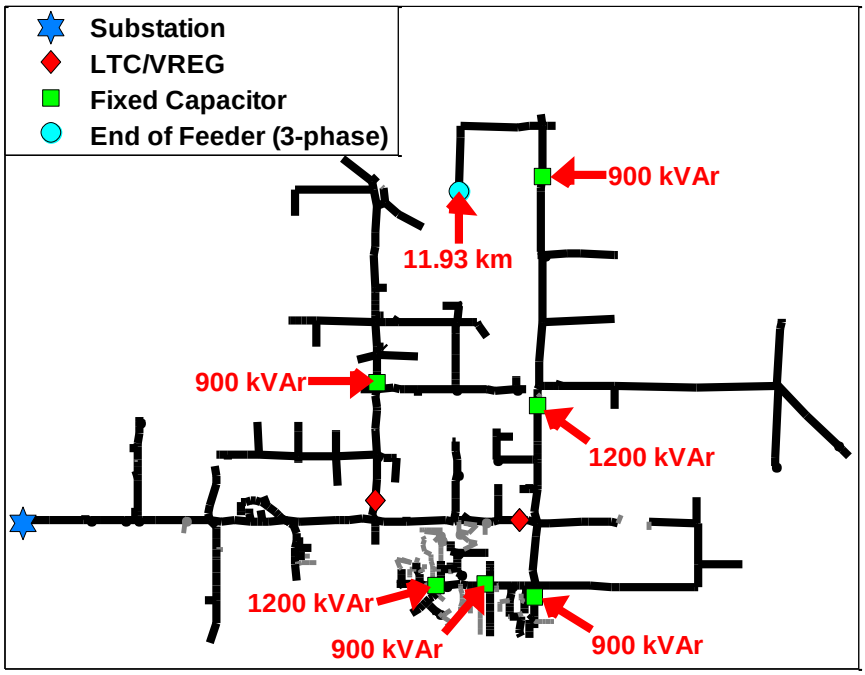


Figure 115. Feeder QS1 circuit diagram.

Figure 116 shows the voltage profile for feeder QS1 without PV at the maximum and minimum daytime load period. In Figure 116, all voltage regulation equipment, including capacitors, have been forced to the top of their band. To conserve space, the bottom of band simulations are always part of the analysis, but the figures are not shown. For QS1, the bottom of band simulation results in similar voltage profiles as those shown in Figure 116, except they are 1.69 V lower on average.

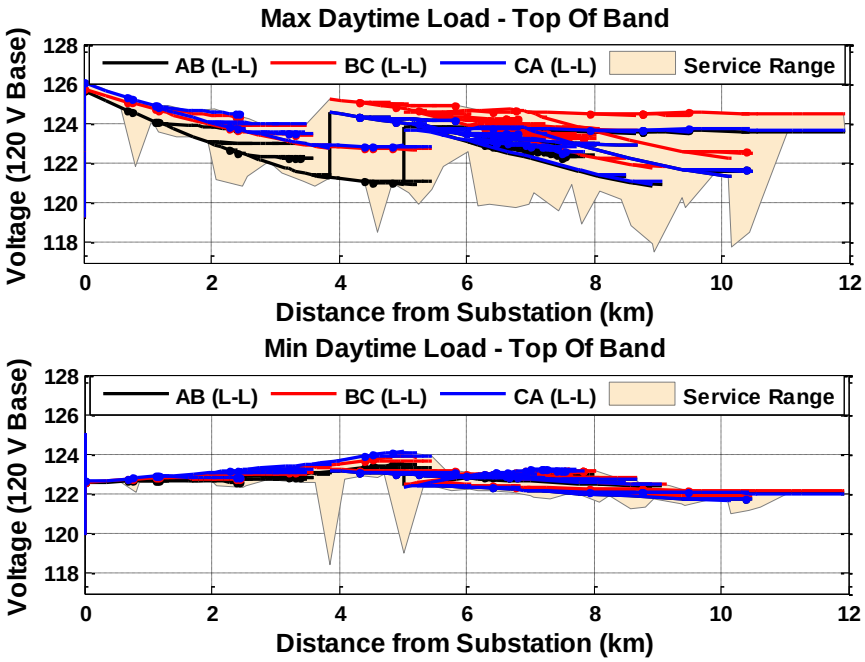


Figure 116. Feeder QS1 voltage profile for the basecase without PV.

The feeder PV impact signature for QS1 is shown in Figure 117 and Figure 118. These types of figures were described in more detail in Section 5.3 and Section 5.7. Figure 117 shows the number of scenarios (PV interconnection locations) at each size that create each type of violation. For example, on QS1, 25% of 4 MW PV interconnection locations would cause a transformer to be overloaded, 65% of 4 MW PV interconnections would cause an over-voltage, 73% would cause a line to be overloaded, and 90% of any 4 MW PV interconnections would cause some issue on the feeder. Figure 118 demonstrates the same sort of analysis using regions with over and under-voltage grouped into the yellow region of only voltage issues that could be mitigated easily. The orange region includes overloaded line or transformers that would be much more costly to mitigate.

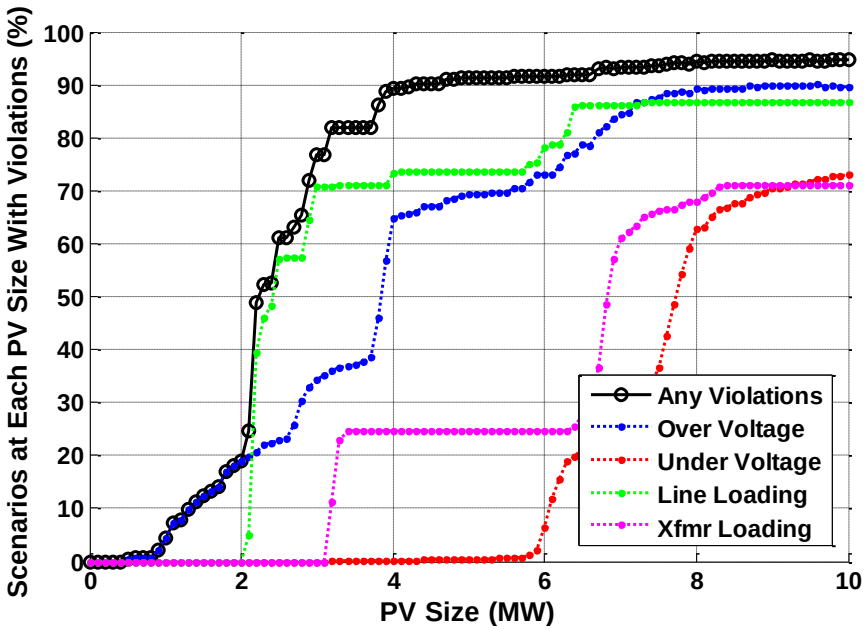


Figure 117. Feeder QS1 PV impact signature for each violation.

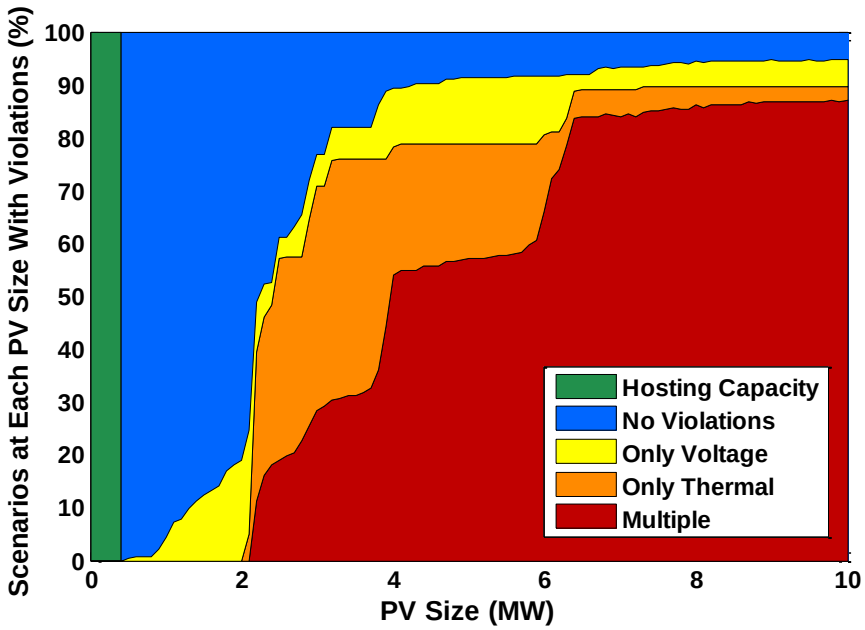


Figure 118. Feeder QS1 PV impact signature with regions.

Figure 119 shows the locational hosting capacities of QS1 marked by the type of violation that is limiting the locational hosting capacity at that bus. For example, the upward-pointing triangles marking over-voltages are generally at the end of the feeder.

The color of each marker is the maximum amount of PV that can be interconnected at that location without causing any issues.

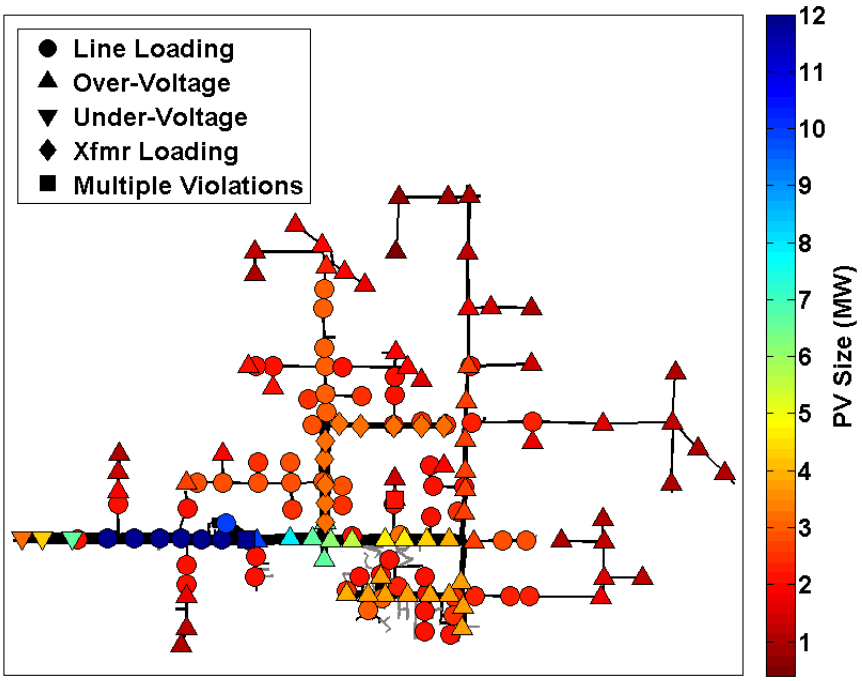


Figure 119. Feeder QS1 locational hosting capacity.

The locational hosting capacities shown in Figure 119 can be analyzed and grouped into what caused the violation. Figure 120 shows a histogram of the violation type determining the locational hosting capacities for QS1. This is essentially a chart of the percentage of markers in Figure 119 that are each shape. The diagonal strips also show if locational hosting capacity at that bus was limited during the minimum or maximum peak load time. For example, any bus where the locational hosting capacity is limited by line overloads almost always occurs during the minimum daytime load period because the reverse current due to the PV injection is higher when the feeder load is lower.

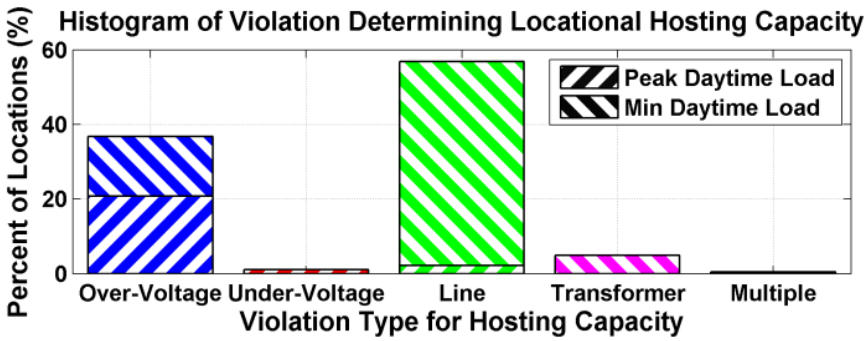


Figure 120. QS1 histogram of violation type determining the locational hosting capacity at each bus.

Figure 121 presents a histogram of the size of the locational hosting capacities in QS1. This is essentially the percentage of markers in Figure 119 that are each color. The histogram in Figure 121 is also colored to show which violation caused the locational hosting capacity to be that size. For example, all buses with the small locational hosting capacities around 1 MW were caused by over-voltage violations.

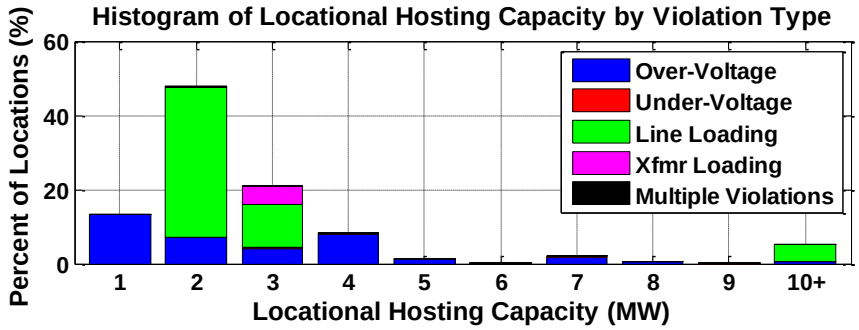


Figure 121. QS1 histogram of the size of the locational hosting capacity throughout the feeder.

These figures are shown in Appendix B for each of the 50 feeders. The results are summarized in Figure 122 through Figure 125. Note that each figure is grouped by voltage class and that the maximum PV size varies. The color contour shows the percent of PV scenarios at each PV size that cause any violations on the feeder. The color scale corresponds to the black line in Figure 117.

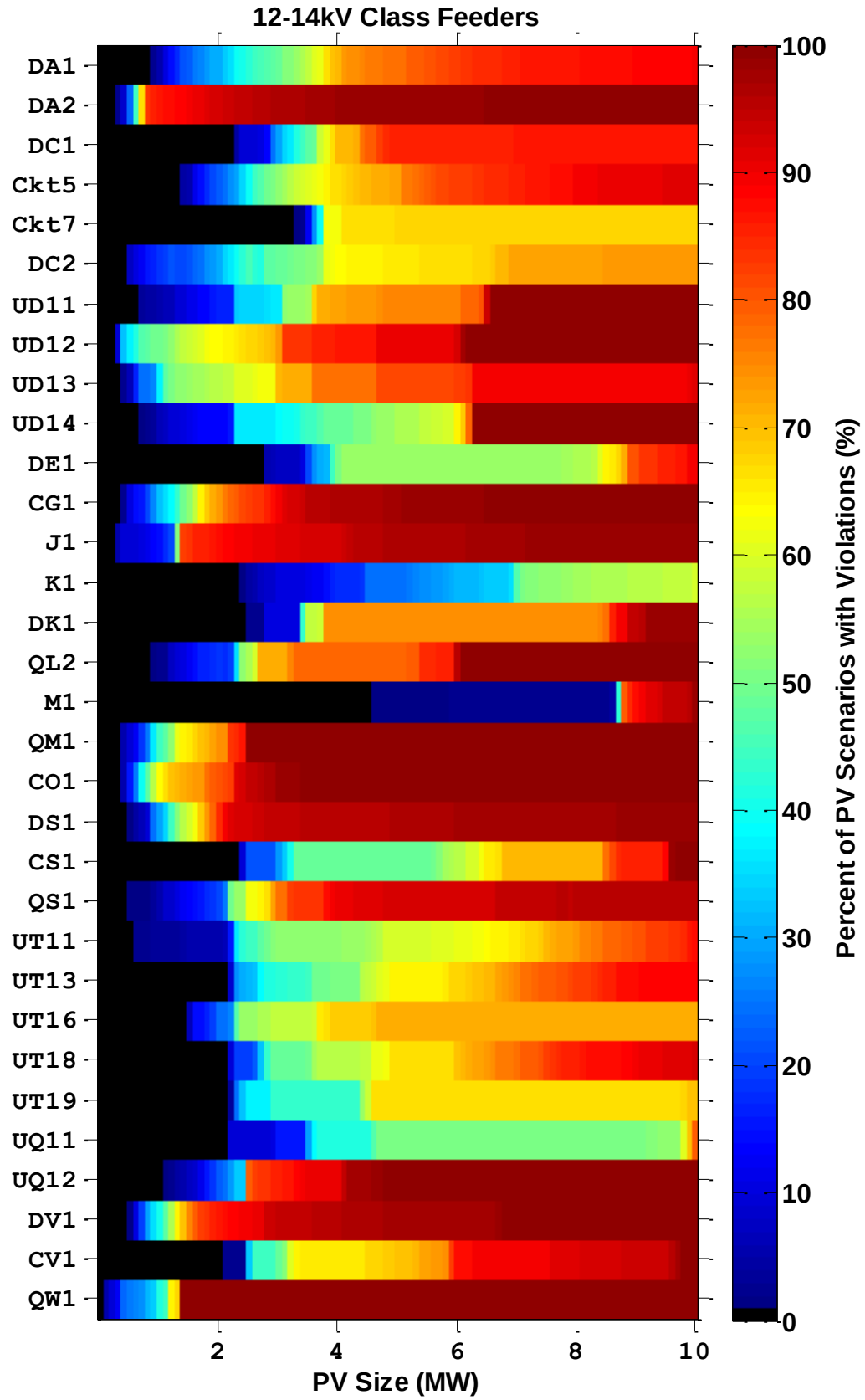


Figure 122. Percent of PV scenarios with violations for the 12-14 kV feeders.

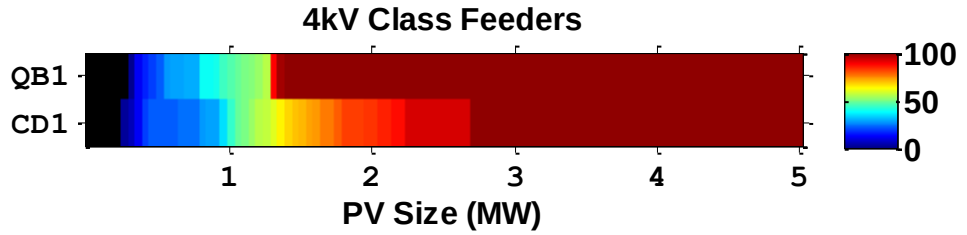


Figure 123. Percent of PV scenarios with violations for the 4 kV feeders.

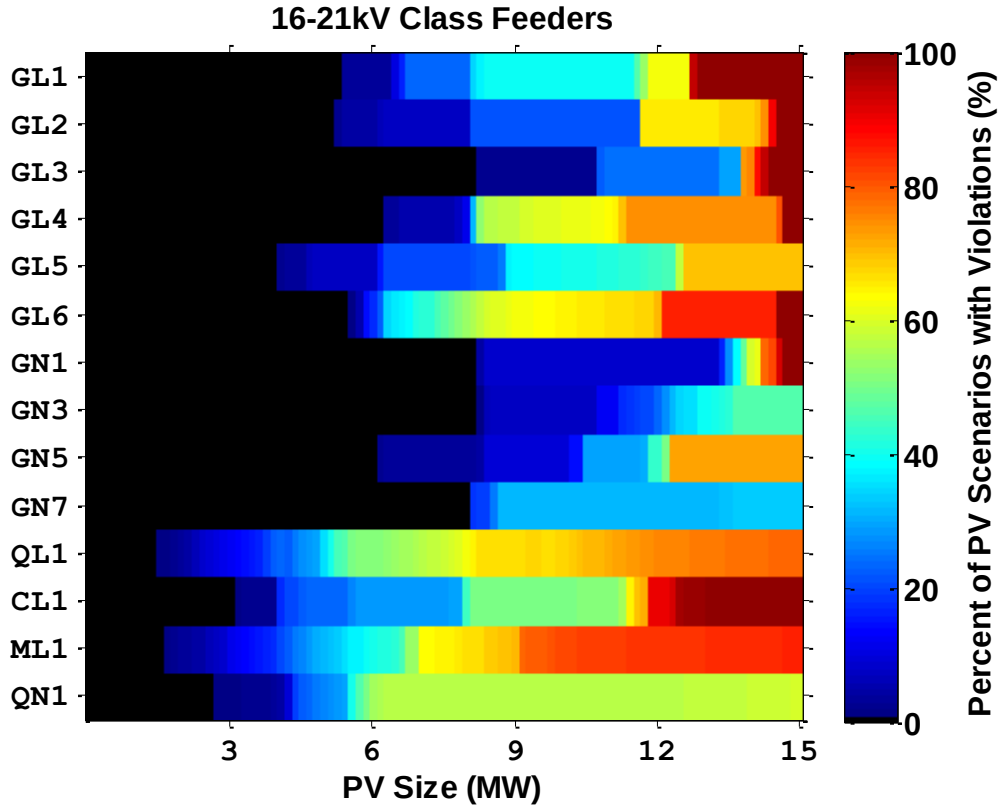


Figure 124. Percent of PV scenarios with violations for the 16-21 kV feeders.

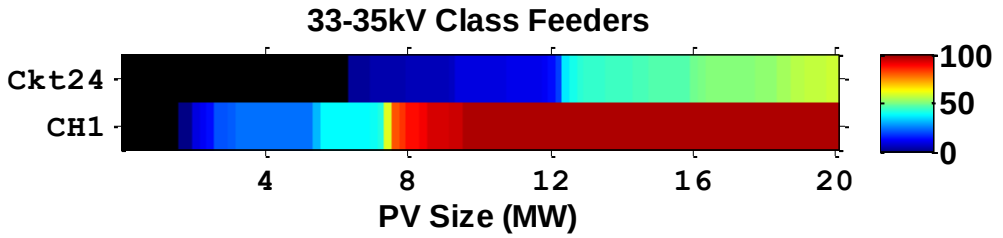


Figure 125. Percent of PV scenarios with violations for the 33-35 kV feeders.

5.10 Technical Evaluation of the 15% of Peak Load PV Interconnection Screen

Many utilities use a standard small generator interconnection procedure (SGIP) process for PV that includes a screen for placing requests on a fast track that do not require more detailed study [3, 63, 64]. One common interconnection screening threshold (IST) is the 15% of peak load screen that fast tracks PV below a certain size. This section includes a technical evaluation of the screen compared to a large number of simulation results for PV on 30 different feeders. Three error metrics are developed to quantify the accuracy of the screen for identifying interconnections that would cause problems or incorrectly sending a large number of allowable systems for more detailed study.

Previously very little work has been done to research and perform technical evaluation of the interconnection screening methods. In [156], 100 small generator interconnection procedure (SGIP) studies were analyzed to determine if PV caused adverse impacts on the electric power system. In [86, 157], EPRI compared the minimum hosting capacity of 18 feeders to the IST. This paper expands on that concept to a larger number of feeders and develops qualitative metrics for calculating the accuracy of the screening methods. Metrics will also be introduced to not only compare the screen to the feeder's minimum PV hosting capacity, but also analyze the distribution of the feeder's locational hosting capacity and the number of violations and false-positives that the screen allows.

A large number of potential PV scenarios (combinations of PV size and location) are investigated using the hosting capacity methodology previously described in [136, 137] to determine if there is any impact to the operation of the distribution system. Simulations are performed for a range of potential feeder load values that occur during daytime hours of 10am to 2pm in the year [63]. With the detailed simulations, it is known if a particular PV interconnection could potentially cause issues to the operations

of the feeder during the year. Each bus has a locational hosting capacity for how much PV can be put at the bus before violations occur. Finally, each feeder has a PV hosting capacity (HC) of the largest PV that can be interconnected anywhere on the feeder without causing issues.

A subset of the database of feeders from the previous section has been analyzed to validate that the 15% of peak load screen is not specific to only one feeder or only specific types of feeders. For this analysis, 30 feeders from various utilities around the United States were simulated using the detailed methodology described in the previous section. The 30 feeders range in length from 1.8 km to 20.3 km. The number of buses in each feeder also varies significantly from 168 buses to 6001 buses per feeder. The range of voltage classes is shown in Table 18. The number of capacitors and regulators per feeder is shown in Figure 126.

Table 18. Feeder Voltage Classes

Voltage Level (kV)	4	12	12.47	13.2	19.8	20.78	34.5
Number of Feeders	1	8	16	1	1	2	1

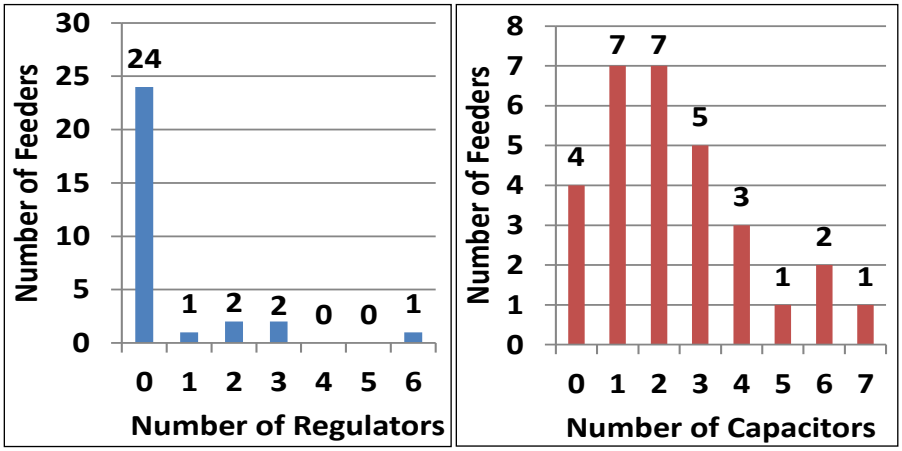


Figure 126. Characteristics of the 30 study feeders.

In order to calculate the accuracy of the 15% of peak load screen, metrics must be defined for comparison between the PV scenarios (sizes, feeders, and locations) that do

not cause problems and the interconnection screen threshold (IST). The motivation for each error metric is explained and example calculations are provided. Figure 127 and Figure 128 are only for demonstration the analysis metrics and are not reflective any one distribution feeder or screening threshold.

The first metric investigates how close the IST is relative to the hosting capacity (HC) for each feeder. Both the IST and HC vary significantly between feeders. A screen accuracy ratio (SAR) of the two numbers will be used to determine the closeness of the screen to the first PV size that could potentially cause issues, equation (35). This number could be positive or negative, and the optimal value is near zero. It is similar to a percent error with respect to the IST for how far it is above or below the HC. This is demonstrated in Figure 127 where the SAR≈70%, meaning the IST could be raised by 70% for this example system.

While SAR provides information about the interconnection screen's accuracy to the feeder hosting capacity, it does not represent how many potentially allowable interconnections (PAI) should have been passed by the screening method because they would not cause any issues. These false positives in the screening process provide the motivation for more accurate screening methods that detect interconnections without violations beyond the allowed interconnections (AI). A large PAI means that the screen is sending a larger number of interconnection requests to a more detailed study than is necessary. Both the AI and PAI are essentially areas calculations as shown in Figure 127. The potential percent increase (PPI) is a ratio of PAI to AI that shows the dramatic number of PV interconnection that could have been allowed by the screen relative to the number that it currently allows, equation (36).

$$SAR = \frac{HC - IST}{IST} * 100 \tag{35}$$

$$PPI = \frac{PAI}{CAI} * 100 \tag{36}$$

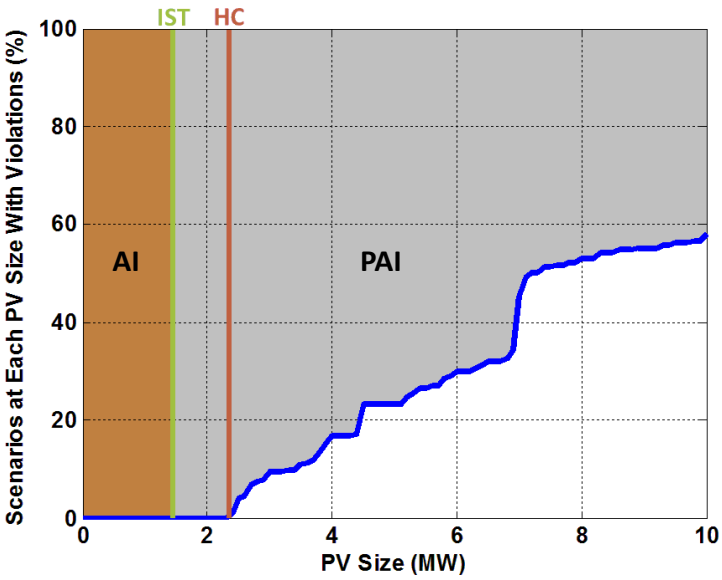


Figure 127. Example of an interconnection screen threshold (IST) with many potential allowable interconnections (PAI) beyond the allowed interconnections (AI).

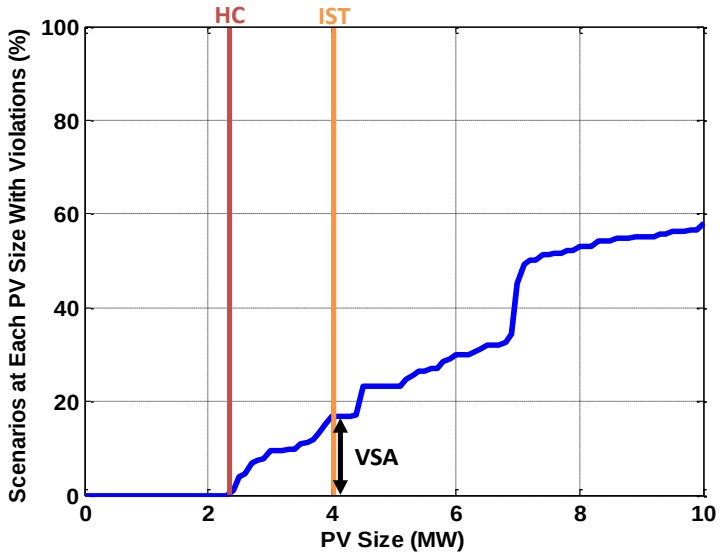


Figure 128. Example of an interconnection screen threshold (IST) that passes PV systems that cause violations the screen allowed (VSA).

The final metric is only used when the IST is too high. When this occurs, the screening criteria will pass potential PV interconnections that will cause violations on the feeder. This metric is simply the number of violations the screen allowed (VSA) as shown in Figure 128. For this case, the SAR is negative.

The screen accuracy ratio (SAR) is calculated individually for each of the 30 feeders. The potential percent increase (PPI) and the violations the screen allowed (VSA) are calculated for all feeders together. For example, the 30 feeders have a total of 10,120 buses for potential PV placement. The VSA is the percent of all 10,120 buses that, when connected with the maximum PV size allowed by the screen at that particular bus, will result in issues on the feeder.

The detailed analysis was performed for all 30 feeders to determine the first PV size that caused issues on the feeder, or the feeder hosting capacity. The results are compared to the 15% of peak load PV IST. These two numbers for each feeder are shown in Figure 129. Figure 129 also demonstrates that the feeder hosting capacity is not well correlated with the feeder load.

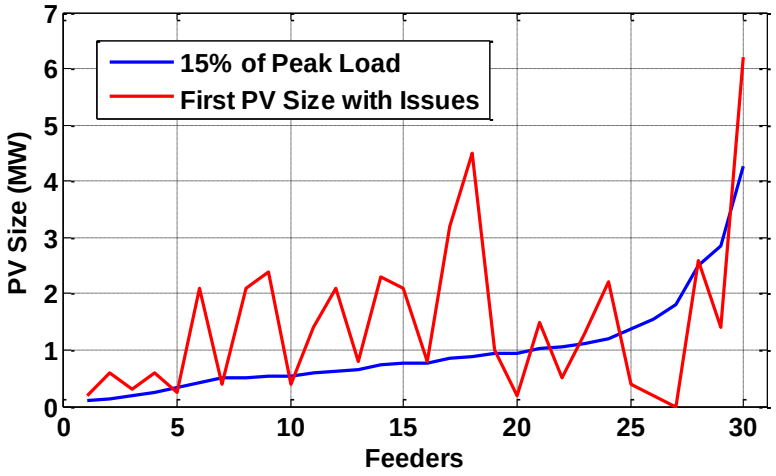


Figure 129. The 15% of peak interconnection screen threshold (IST) and the first PV size with issues (hosting capacity) for each feeder.

The values in Figure 129 are used to calculate the SAR for each feeder. The distribution of SAR errors for the 15% of peak load screen is shown in Figure 130. With a max of SAR=418%, the HC for that feeder is more than 4 times larger than 15% of peak screen. The average is SAR=95%, but there is also a SAR=-95% which means the IST is much higher than the feeder hosting capacity.

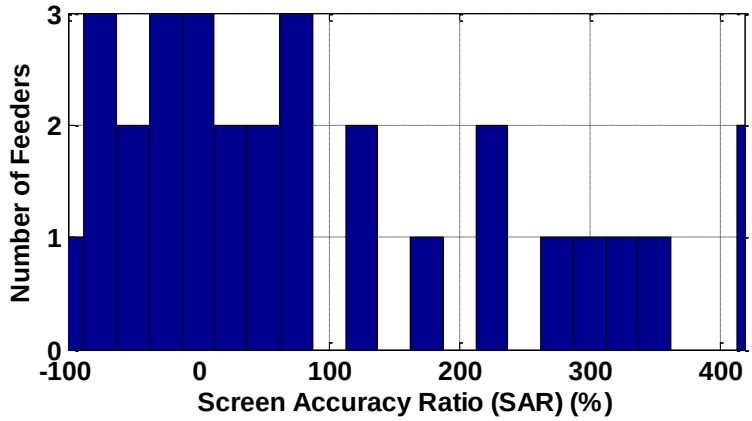


Figure 130. The screen accuracy ratio (SAR) error distribution for the 15% of peak and minimum daytime load screens.

The feeders with negative SAR values result in passing a certain number of PV interconnections that will cause operational problems on the distribution system. The violations the screen allowed (VSA) are shown in Figure 131. Placing the maximum PV size allowed by the 15% of peak load screen randomly on one of the 10,120 buses of the 30 feeder will result in issues 16.6% of the time. The screen is obviously not conservative enough in certain cases and is passing PV interconnections that require a more detailed interconnection analysis.

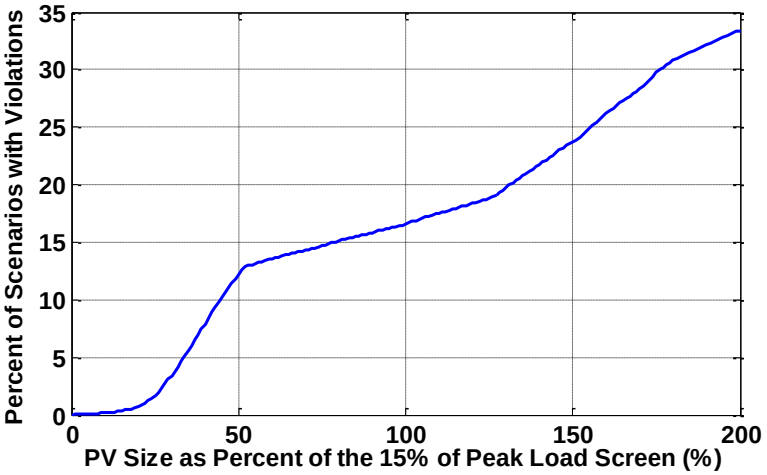


Figure 131. Violations the screen allowed (VSA) for the 15% of peak load interconnection screen threshold (IST).

The potential percent increase is more difficult to show graphically, but the allowed interconnections (AI) and the potentially allowable interconnections (PAI) are totaled up for each of the 30 feeders. For the 15% of peak screen, the potential percent increase (PPI) results in 346% more potential PV interconnections that do not cause violations than are currently passed by the screen.

A novel analysis is presented for the accuracy of the 15% of peak load PV interconnection screen compared to wide range of PV scenarios on 30 different real distribution feeders. The qualitative accuracy of screening methods has not been previously well studied, especially for a large database of feeders. Three new error metrics were developed to quantify the accuracy of the screening method for identifying interconnections that would cause problems or incorrectly sending a large number of allowable systems for more detailed study

With a SAR=95%, the 15% screen on average is twice as high as the minimum PV size that will cause any issues. The VSA=16.6% demonstrates though that the screen is passing a considerable percentage of interconnections that could cause problems. Finally, PPI=346% shows the significant potential for improvement in more advanced screening methods.

CHAPTER 6: CONCLUSIONS AND FUTURE RESEARCH

6.1 Conclusions

This thesis includes advanced computational methods for analyzing potential impacts of high penetration PV on the distribution system, which can be used to streamline the PV interconnection process. More accurate methods are developed that require less time for both the PV interconnection screening criteria and the PV interconnection impact study process.

A timeseries analysis approach is shown to more fully capture the time-varying nature of solar energy and the interaction with distribution system operations. The impact of different variability profiles, regulator control algorithms, and smart inverters with volt/var functionality are all demonstrated in quasi-static time-series (QSTS) simulations. QSTS is only going to become more critical as higher penetrations of PV are reached. It will be important to understand how solar variability propagates throughout the feeder and how each individual smart inverter operates together at different times of year and during certain events.

Because extended high-resolution QSTS simulations require long computation times, an equivalent circuit reduction method was developed to simplify the circuit to a reduced order model. The reduced circuit is equivalent during timeseries simulations, but it solves in a fraction of the time. The algorithm works with unbalanced multi-phase complex distribution system models, and it has been shown to have high accuracy when validated against the full models.

An advanced PV hosting capacity simulation tool is developed and used to quantify system impacts for many PV interconnection scenarios, configurations, and locations, which can be generalized to develop improved future interconnection screening criteria. The advanced tools quantify location-specific impacts and the locational hosting

capacity of potential PV interconnection locations on the feeder, including PV impact signatures and zones. A set of 50 different real distribution systems is analyzed in detail to demonstrate the range of scenarios and impacts that can occur depending on the feeder characteristics and topology.

Specific methods are developed for time-series analysis, faster simulation times, distribution system equivalent circuit reduction, and PV hosting capacity analysis. The advancements presented in this thesis assist in streamlining PV interconnection studies with faster interconnection analysis times and more accurate screening criteria.

6.2 Summary of Contributions

Related to the work presented in this thesis, there have been 5 journal publications [132, 158-161], 18 conference publications [1, 5, 35, 54, 55, 68, 89, 136, 137, 152, 154, 162-168], and 6 technical reports [13, 73, 121, 151, 169, 170] accepted or submitted.

During the time at Georgia Tech, Matthew Reno was also involved in 2 additional journal paper [171, 172] and 4 conference papers [173-176] not related to research in this dissertation. Several awards were received for this work, including best poster presentation (2013) and best student paper (2014) at IEEE Photovoltaic Specialists Conference.

In summary, the primary contributions of the work are:

- Demonstration of a timeseries analysis approach for modeling PV impacts on the distribution system.
- Analysis of the interaction between solar variability and voltage regulation equipment for various PV variability profiles, simulation parameters, and voltage regulator control settings in order to determine the impact to the number of tap change operations.
- Simulation of smart inverters with volt/var functionality in quasi-static time-series (QSTS) simulations.

- Demonstration of improved computational methods for increasing the speed of QSTS analyses.
- Development of a circuit reduction method to reduce very large complex distribution system models to a simpler, yet equivalent, system.
- Expansion of the circuit reduction methodology to apply to more realistic distribution systems with unbalance, mutual line impedances, line charging capacitance, and transformers with core losses.
- Implementation of the circuit reduction algorithm in MATLAB and application to several large distribution systems to validate accuracy and consistency.
- Development of advanced simulation methods for PV interconnection analysis to quantify location-specific impacts and the locational hosting capacity of potential PV interconnection locations on the feeder.
- Expansion of the analysis tool to include improved modeling of voltage regulation equipment, including all potential regulator states and any temporary over-voltage (TOV) conditions from PV ramping events.
- Demonstration of the response of entire distribution feeders to PV through impact signatures and zones.
- Analysis of 50 different real distribution systems to demonstrate the range of scenarios and impacts that can occur depending on the feeder characteristics and topology.

6.3 Recommended Future Work

The computational speed of QSTS simulations should continue to be improved. New innovative methods for advanced time-series analysis should be developed, such as event-based simulations, linear power flow approximation, parallel processing of power

flow solutions separable by time, and state-based time-series. Given that the focus of timeseries simulations is often events, such as regulator tap changes, performing event-based simulations that do not solve every second during the year would provide a significant improvement in speed. In Section 3.8, a state-based timeseries solution was proposed for approximating the number of tap changes in a year very quickly. The state-based timeseries should continue to be expanded to ensure that it can be applied to large feeders with many different switching capacitors and regulators.

The circuit reduction methods should be expanded to systems with various load profiles and PV output profiles. It should be straightforward to incorporate groups of loads, such as if all residential customers are following the same profile. The more complicated future work would investigate how to aggregate distributed PV systems with smart inverter functionality. It was shown that distributed PV can be easily reduced into only a couple PV systems, but when using the reduction methods shown, any circuit component that measures the voltage becomes a bus of interest. With hundreds of distributed PV systems with volt/var control on a feeder, a method will need to be developed to produce an aggregate PV system that still provides equivalent volt/var output during a timeseries simulation.

The hosting capacity analysis should be expanded to include analysis for impacts to the feeder protection scheme, such as under-reach, sympathetic tripping, and coordination [162]. The improvement in hosting capacity from adding volt/var control to PV inverters should also be investigated [89]. Future work could also include expanding the database of analyzed feeders to increase the sample size. Future analysis will continue to study the correlation between the hosting capacity results and feeder characteristics in order to determine the most important interconnection screening criteria. The results could also be used to determine the best way to cluster feeders in a utility in order to apply more generic evaluations based on studying a few representative feeders [177].

APPENDIX A: GRIDPV TOOLBOX OVERVIEW

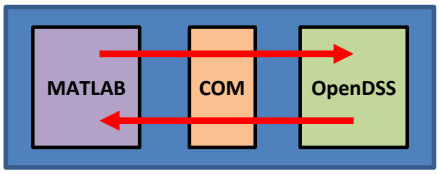
As a result of the work presented in this dissertation, an open-source MATLAB toolbox was created for interacting with OpenDSS and modeling PV on the distribution system. This toolbox is available online, and the full documentation is provided in [169]. The majority of the functions are useful for interfacing OpenDSS and MATLAB, and they are of generic use for commanding OpenDSS from MATLAB and retrieving information from simulations. A set of functions is also included for modeling PV plant output and setting up the PV plant in the OpenDSS simulation. The toolbox contains functions for modeling the OpenDSS distribution feeder on satellite images with GPS coordinates. Finally, example simulations functions are included to show potential uses of the toolbox functions. Each function in the toolbox is documented with the function use syntax, full description, function input list, function output list, example use, and example output.

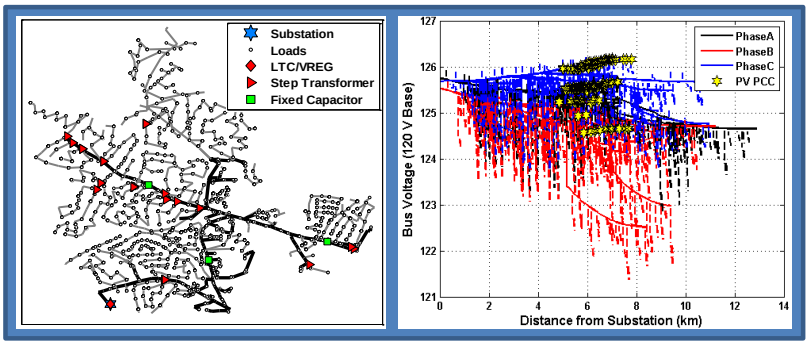
OpenDSS (from the Electric Power Research Institute (EPRI) [117]) is used to model the distribution system with MATLAB providing the frontend user interface through a COM interface. OpenDSS is designed for distribution system analysis and is very good at timeseries analysis with changing variables and dynamic control. OpenDSS is command based and has limited visualization capabilities. By bringing control of OpenDSS to MATLAB, the functionality of OpenDSS is utilized while adding the looping, advanced analysis, and visualization abilities of MATLAB.

GridPV Toolbox is a well-documented tool for Matlab that can be used to build distribution grid performance models using OpenDSS. Simulations with this tool can be used to evaluate the impact of solar energy on the distribution system [136, 137].

Overview of GridPV Features

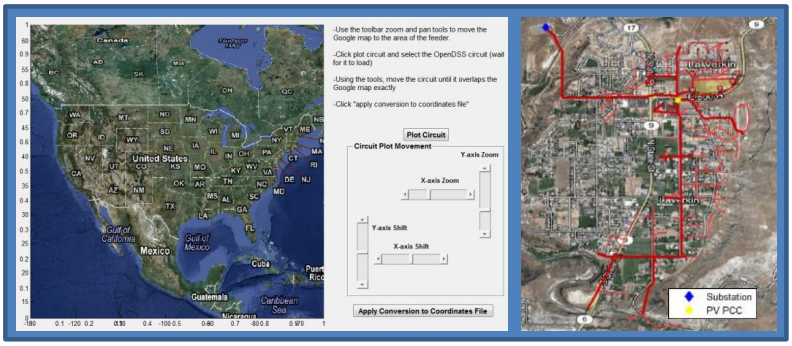
Standardizes interface between MATLAB and OpenDSS for easy parameter queries

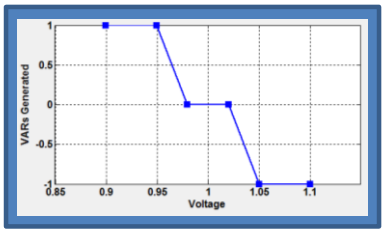




Validates OpenDSS feeders and checks for errors

Integrates GIS functionality through Google Maps and includes functions to convert between coordinate systems

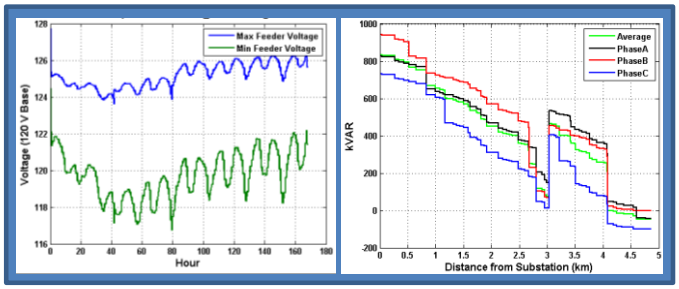


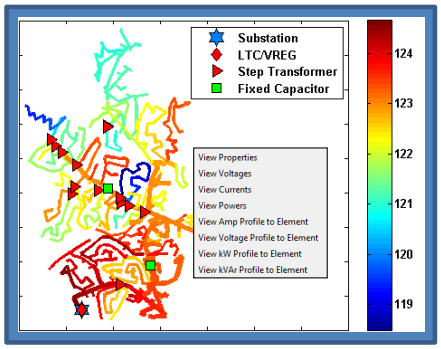


Models solar power easily and accurately

- **GUI for setting up PV plants**
- **Model solar variability for size and dispersion of PV**
- **Power factor and reactive power control for PV plants**
- **Central and distributed plants**

Performs time-series and steady-state simulations





Plots and visualizes results

- **Clean and interactive plots with numerous options**
- **Integrated plotting options such as feeder circuit diagram and voltage, current, and power profiles**

The functions in the toolbox are categorized into five main sections in the manual: OpenDSS functions, Solar Modeling functions, Plotting functions, Geographic Mapping functions, and Example Simulations. Each function is documented with the function use syntax, full description, function input list, function output list, and an example use. The function example also includes an example output of the function.

OpenDSS Functions

DSSStartup - Function for starting up OpenDSS and linking to MATLAB

getBusCoordinatesArray - Gets the coordinates for all buses that have a location in OpenDSS

getBusInfo - Gets the information for all Bus in busNames

getCapacitorInfo - Gets the information for all capacitors in the circuit

getCoordinates - Gets the coordinates for the buses in busNames

getGeneratorInfo - Gets the information for all generators in the circuit

getLineInfo - Gets the information for all lines in the circuit

getLoadInfo - Gets the information for all loads in the circuit

getPVInfo - Gets the information for all PV plants in the circuit

getTransformerInfo - Gets the information for all transformers in the circuit

isinterfaceOpenDSS - Used to check for a valid interface input.

Circuit Analysis Functions

circuitCheck - Used to error-check the circuit for any obvious abnormalities

findDownstreamBuses - Finds all buses downstream of the busName

findHighestImpedanceBus - Finds the highest impedance bus for each phase to the source bus

findLongestDistanceBus - Finds the bus for each phase that is farthest distance away

findSubstationLocation - Locates the substation coordinates

findUpstreamBuses - Finds all buses upstream of the busName

Plotting Functions

plotAmpProfile - Plots the line currents profile and line rating vs. distance

plotCircuitLines - Plots the feeder circuit diagram

plotCircuitLinesOptions - GUI for providing options for how to plot the feeder circuit diagram

plotKVARProfile - Plots the feeder profile for the kVAR power flow on the lines

plotKWProfile - Plots the feeder profile for the kW power flow on the lines

plotMonitor - Plots a monitor from the simulation

plotVoltageProfile - Plots the voltage profile for the feeder (spider plot)

Geographic Mapping Functions

initCoordConversion - Function to initialize the coordinate conversion process

createCircuitCoordConversion - Function to create conversion of circuit coordinates to GPS coordinates

createCircuitCoordConversionUTM - Function to create conversion of circuit coordinates in UTM to GPS coordinates

plotGoogleMap - Plots a Google map on the current axes using the Google Static Maps API

Solar Modeling Functions

placePVplant - Draw PV on the circuit diagram and save plant info for WVM input

createPVscenarioFiles - Runs the WVM model and puts out the OpenDSS PV scenario files

distributePV - Allocates PV based off of the load transformer size (kva)

findMaxPenetrationTime - Finds the max penetration time

IneichenClearSkyModel - Generates the clear sky irradiance using Ineichen and Perez model

makePFoutputFunction - GUI for creating power factor as a function of PV power output

makePFprofile - Creates varying Power Factor profile by schedule or PV output

makePFschedule - GUI for creating a power factor daily schedule

makeVVCcurve - GUI for setting up the OpenDSS VVControl function parameters

pvl_WVM - WVM Wavelet Variability Model

Example Simulations

examplePeakTimeAnalysis - Runs simulation during peak penetration time and generates plots

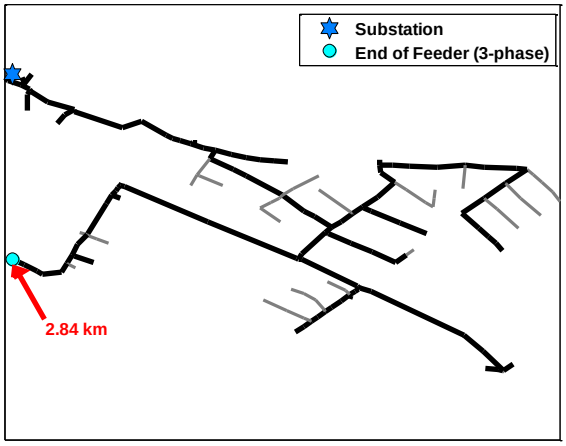
exampleTimeseriesAnalyses - Timeseries analysis and plots monitor values from the simulation

exampleVoltageAnalysis - Example analysis of maximum and minimum feeder voltages through time

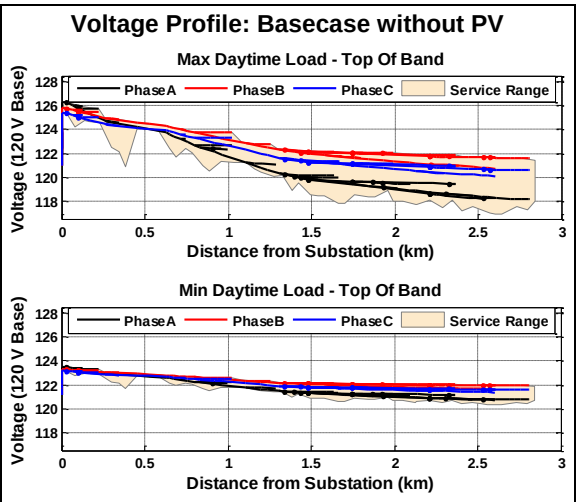
APPENDIX B: HOSTING CAPACITY ANALYSIS OF 50 FEEDERS

In Chapter 5, a methodology for analyzing the PV interconnection impact risk to distribution system operations was presented. This analysis was performed on a range of distribution systems and feeder topologies in order to demonstrate the feeder characteristics that correlate to the impacts caused by PV. Each of the 50 distribution system models analyzed is a real feeder located in the United States. Each model is simulated in full detail, including substation settings, short-circuit impedances, voltage regulation controls, and estimated secondary system parameters. The majority of the feeders included a year of load data that could be used for the analysis. When load data existed, the minimum and maximum peak load that occurred on each feeder during high daytime PV output (10am to 2pm) [63] is used for the analysis. For the two feeders where the load data is unknown (K1 and M1), the average daytime min and max ratio from the other feeders was applied. For details on each of the diagrams for each feeder in Appendix B, see Section 5.9. The feeders are organized in ascending order by voltage level.

QB1

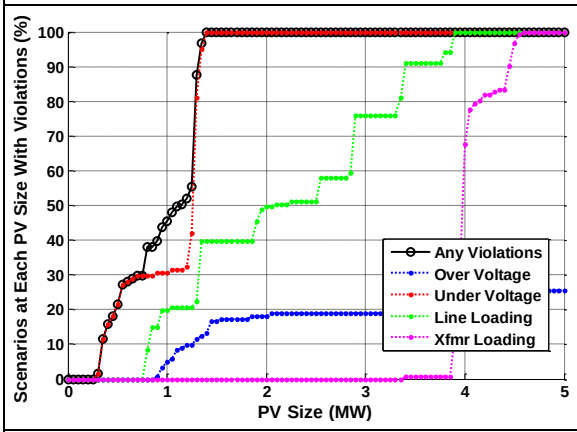


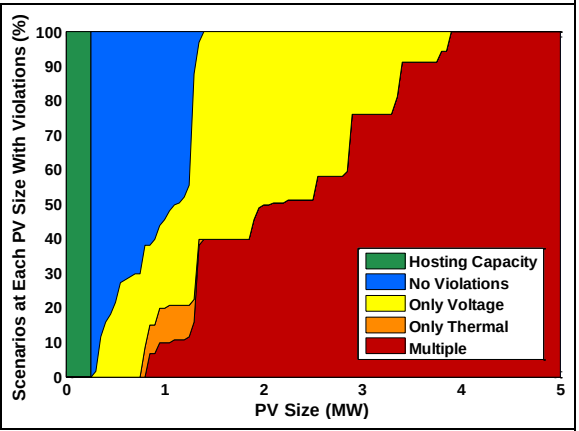
4.0 kV, 2.21 MW peak load
Max daytime load = 1.88 MW (85%)
Min daytime load = 0.63 MW (28%)



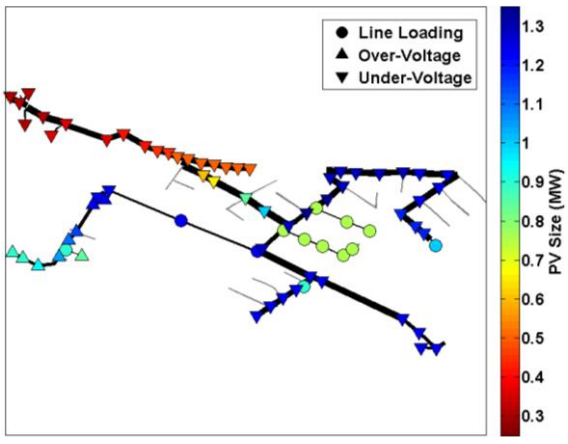
Bottom of Band bus voltages average 1.92V lower

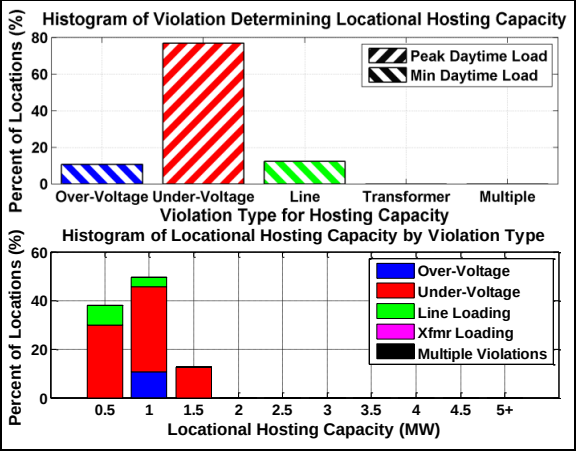
PV Impact Signature



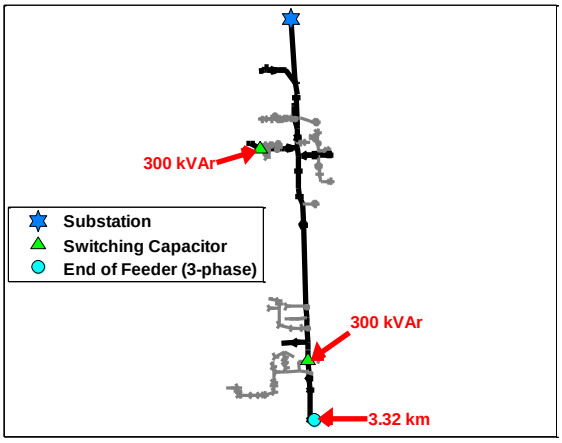


Locational Hosting Capacity



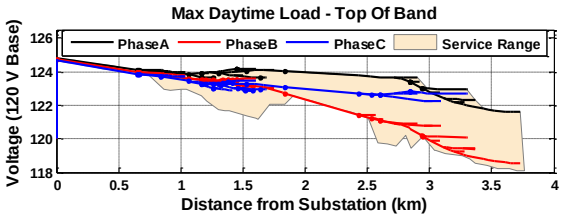


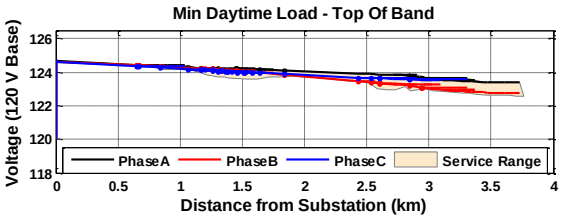
CD1



4.0 kV, 1.84 MW peak load
Max daytime load = 1.62 MW (88%)
Min daytime load = 0.33 MW (18%)

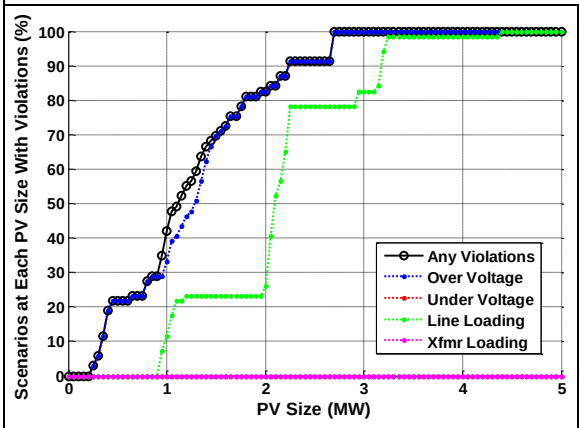
Voltage Profile: Basecase without PV

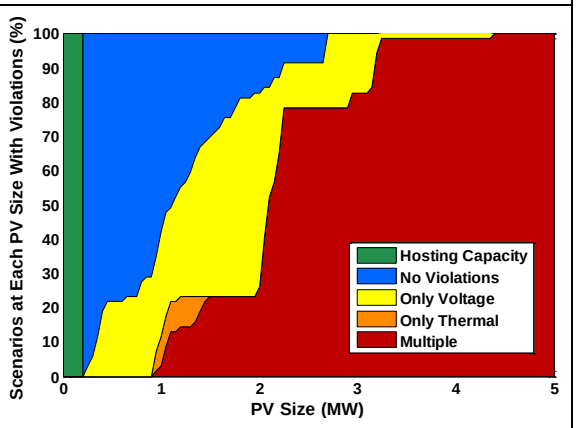




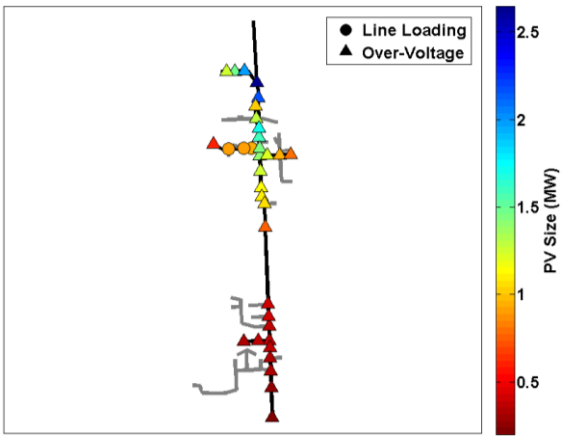
Bottom of Band bus voltages average 1.89 V lower

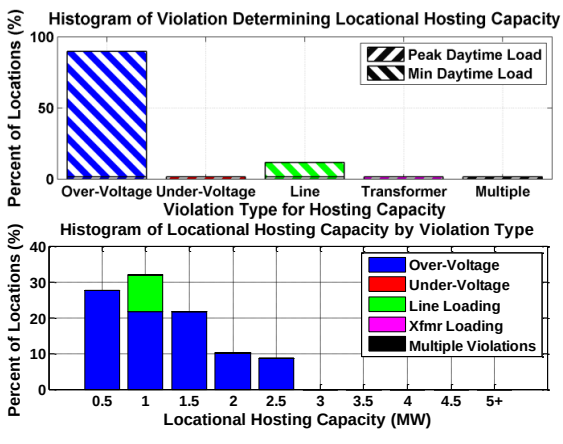
PV Impact Signature



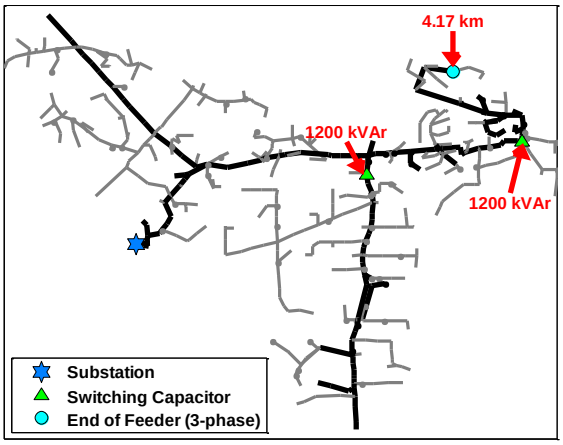


Locational Hosting Capacity

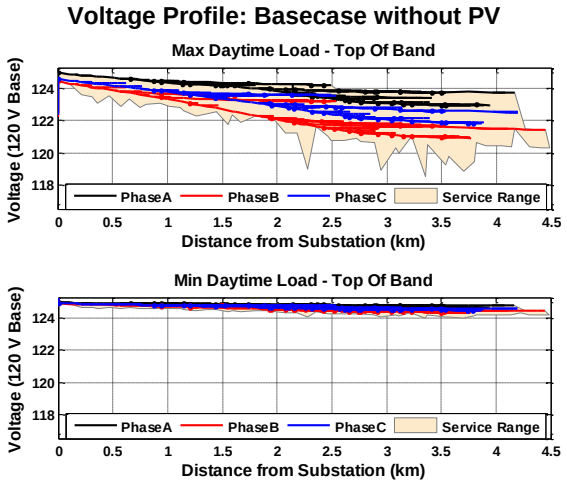




DA1

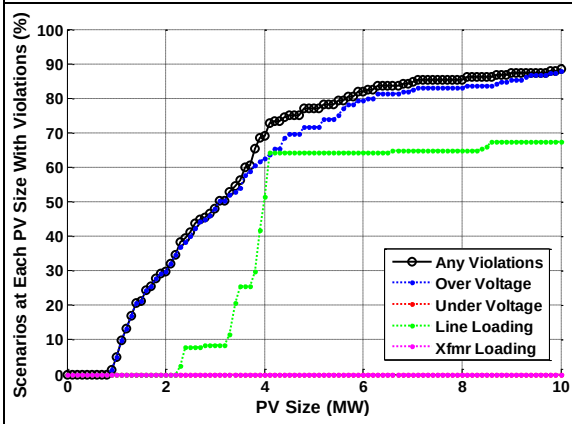


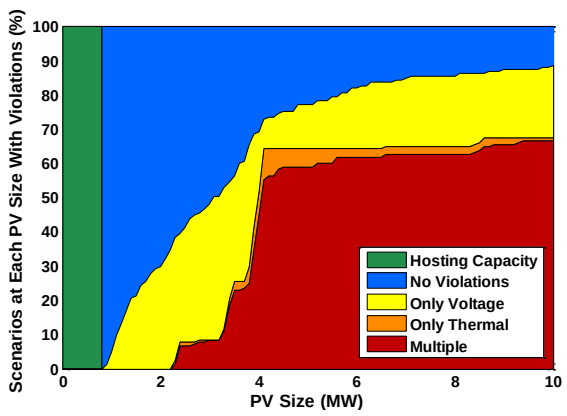
12 kV, 4.43 MW peak load
Max daytime load = 4.37 MW (99%)
Min daytime load = 0.72 MW (16%)



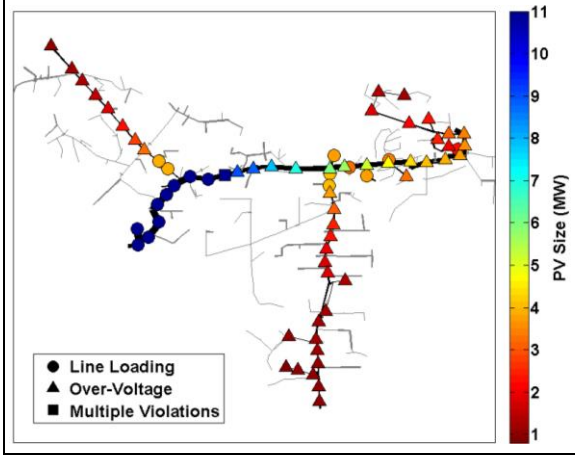
Bottom of Band bus voltages average 3.99 V lower

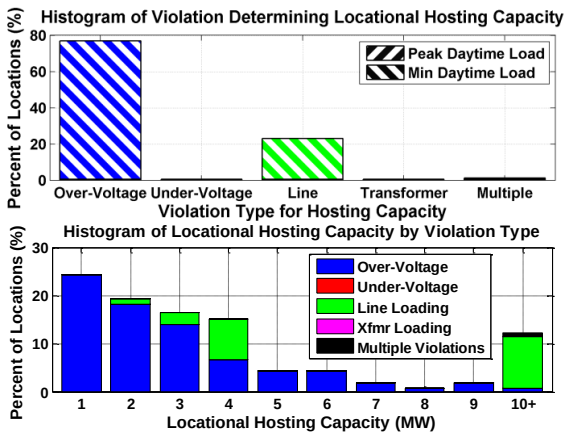
PV Impact Signature



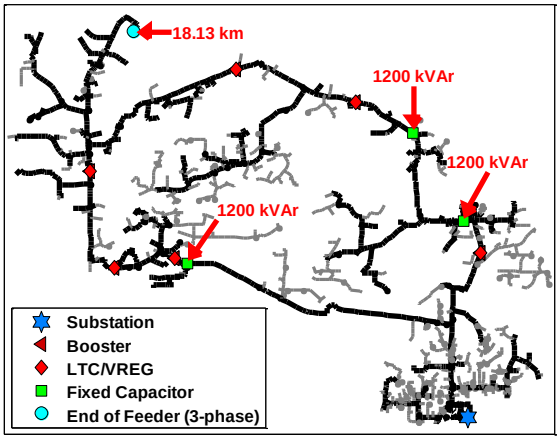


Locational Hosting Capacity

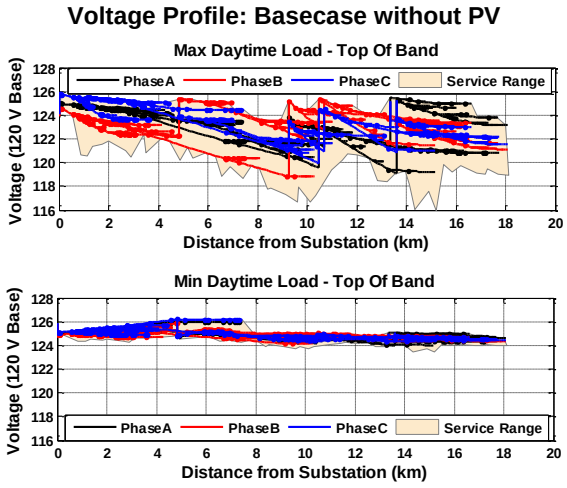




DA2

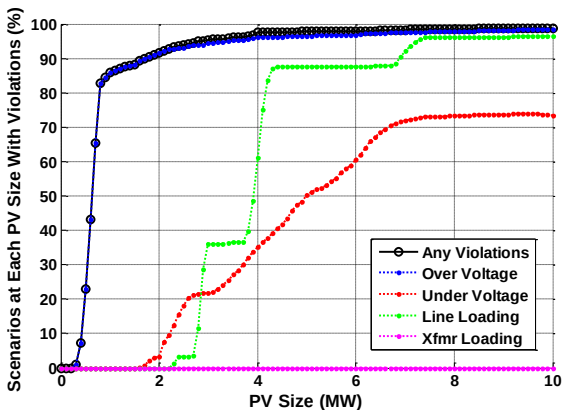


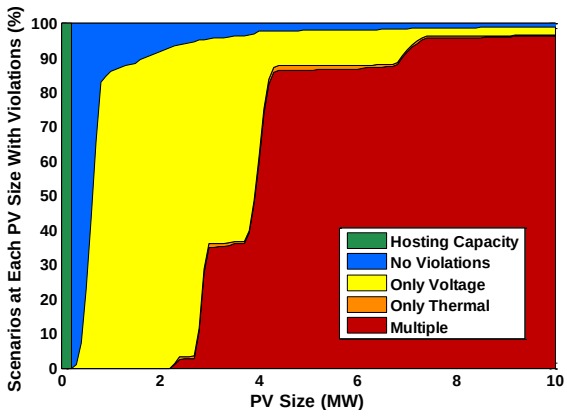
12 kV, 10.35 MW peak load
Max daytime load = 8.93 MW (87%)
Min daytime load = 1.64 MW (16%)



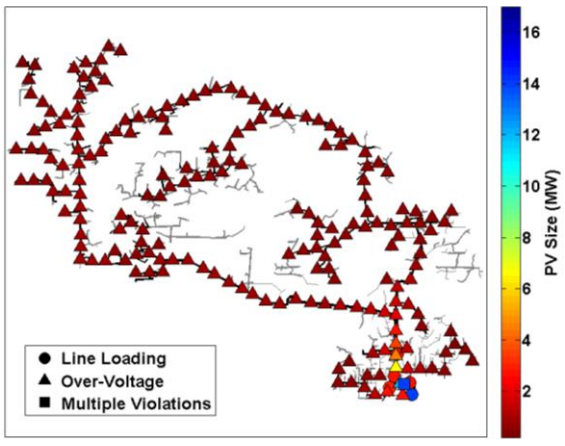
Bottom of Band bus voltages average 4.08 V lower

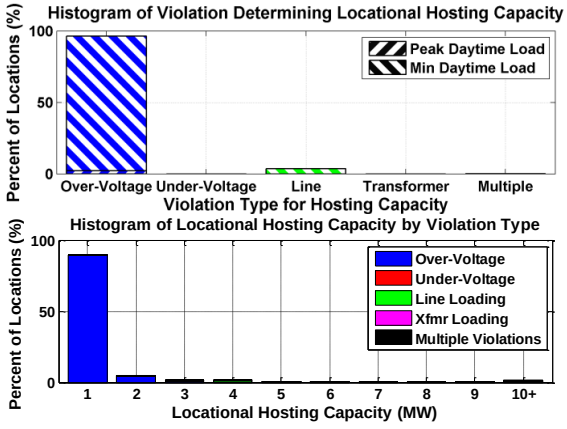
PV Impact Signature



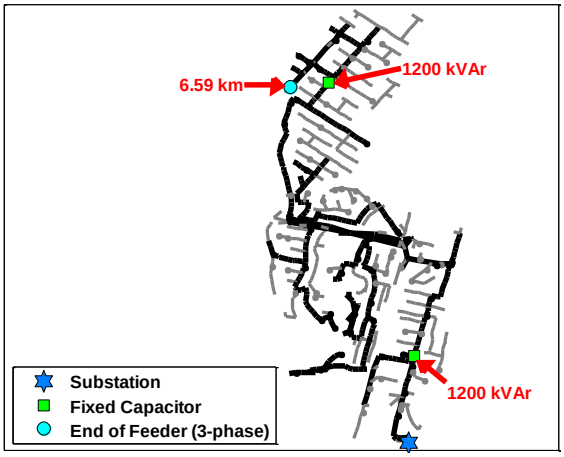


Locational Hosting Capacity

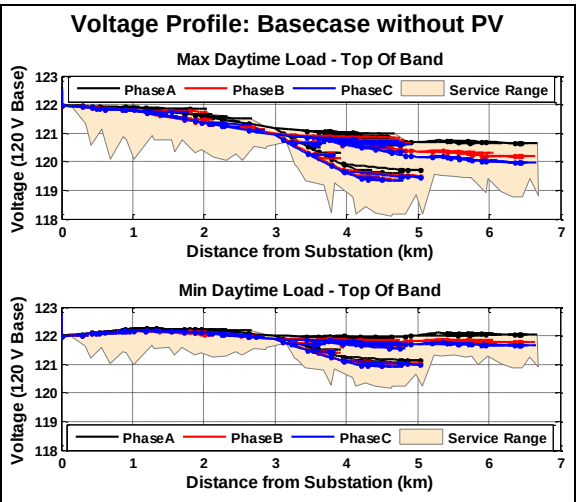




DC1

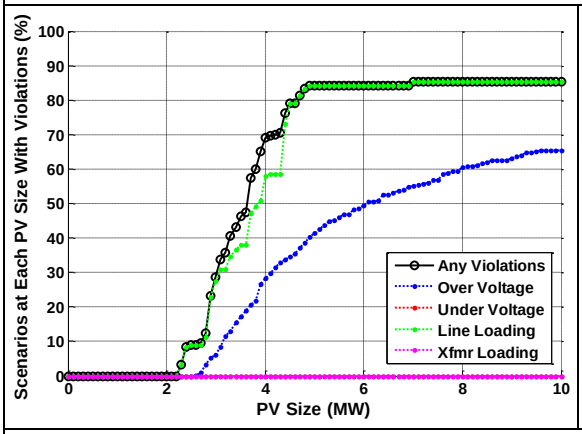


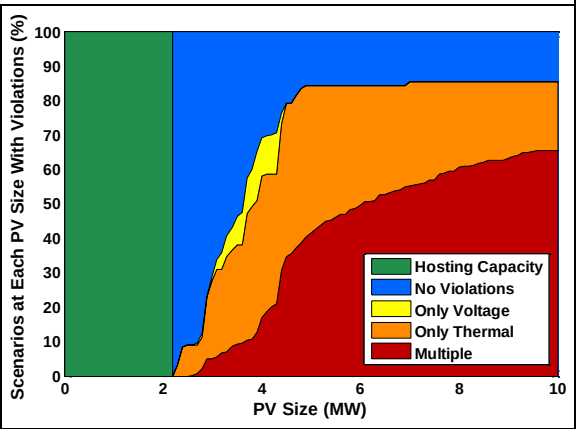
12 kV, 8.08 MW peak load
Max daytime load = 6.14 MW (76%)
Min daytime load = 3.70 MW (46%)



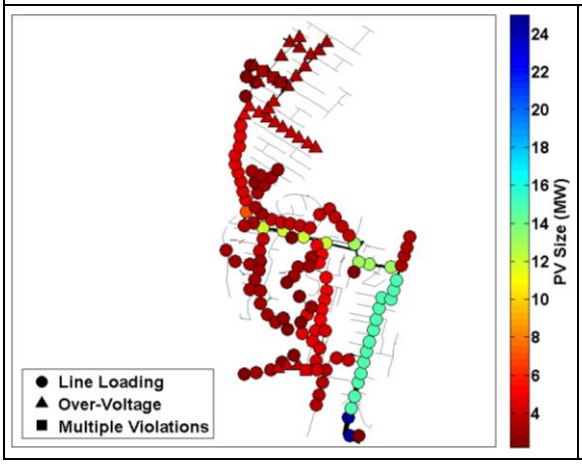
Bottom of Band bus voltages average 3.06 V lower

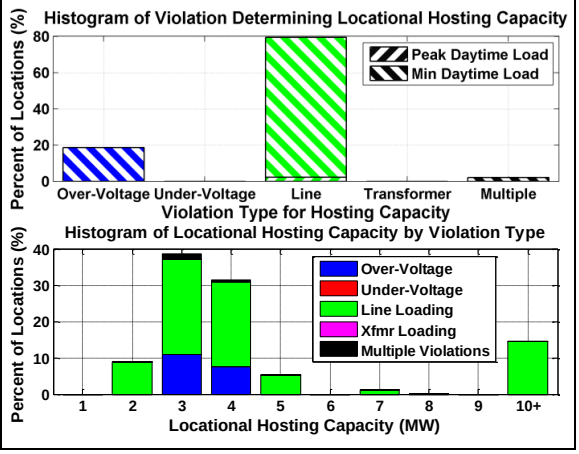
PV Impact Signature



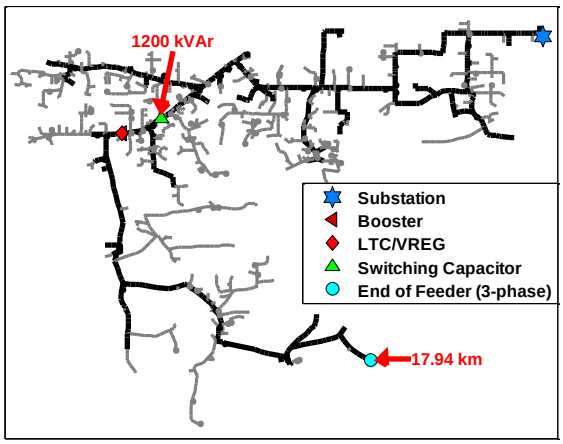


Locational Hosting Capacity

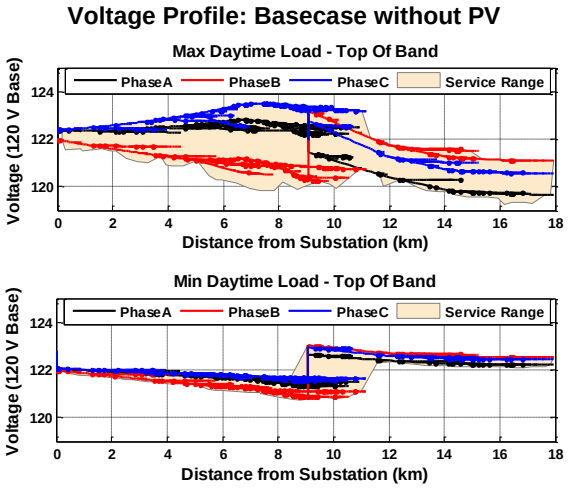




DC2

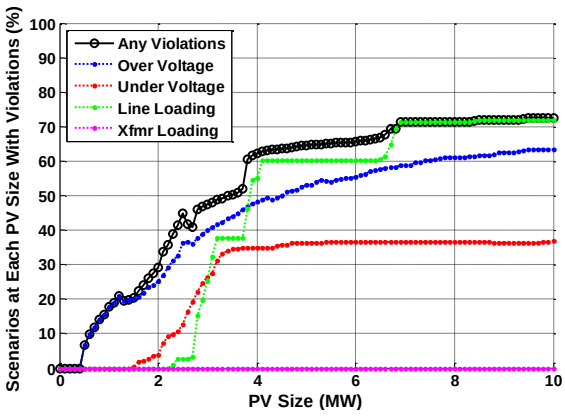


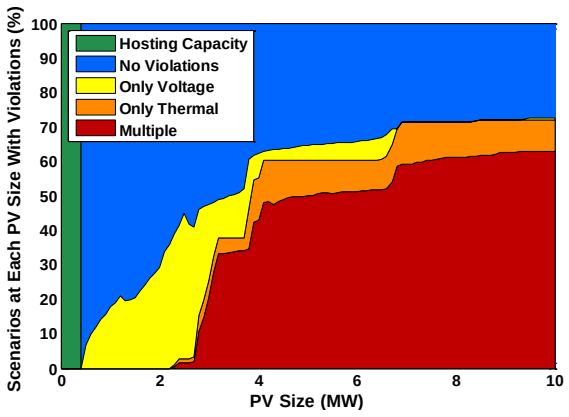
12 kV, 3.60 MW peak load
Max daytime load = 2.55 MW (71%)
Min daytime load = 0.62 MW (17%)



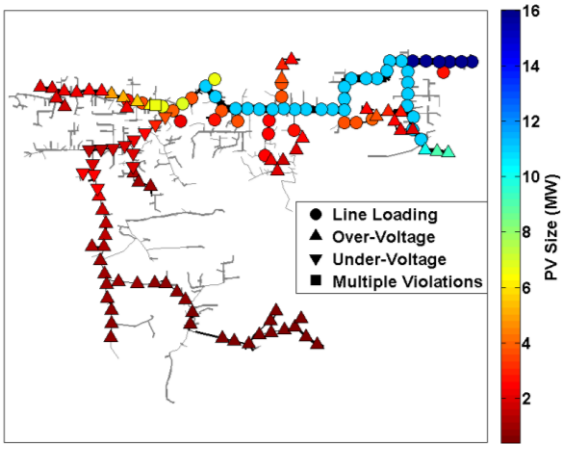
Bottom of Band bus voltages average 2.52 V lower

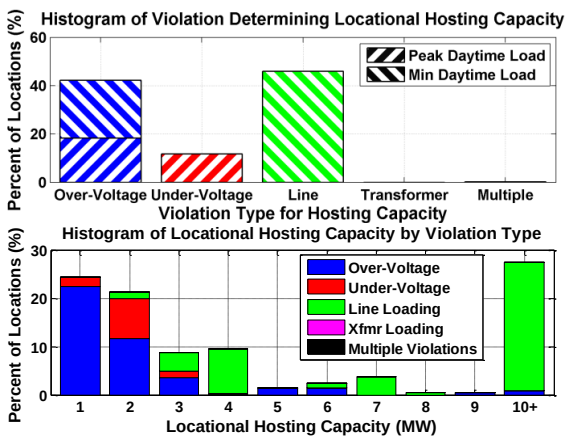
PV Impact Signature



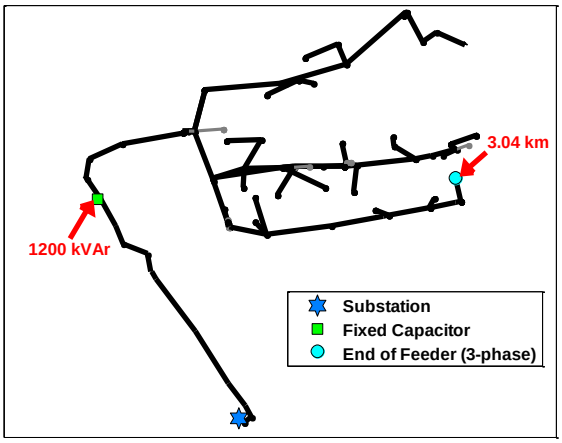


Locational Hosting Capacity



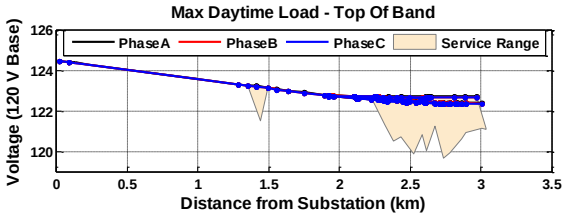


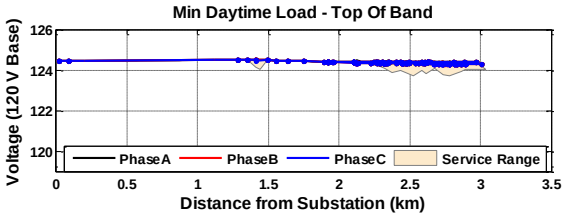
DE1



12 kV, 7.85 MW peak load
Max daytime load = 7.85 MW (100%)
Min daytime load = 1.74 MW (22%)

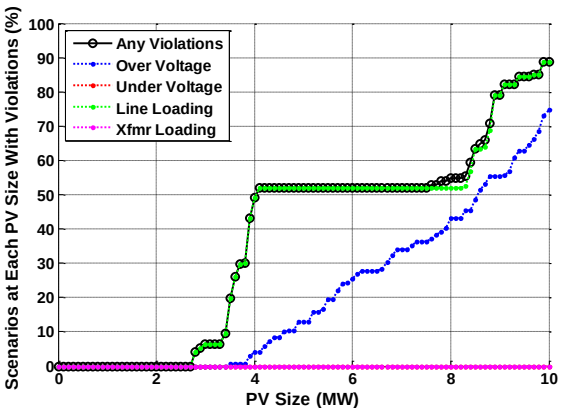
Voltage Profile: Basecase without PV

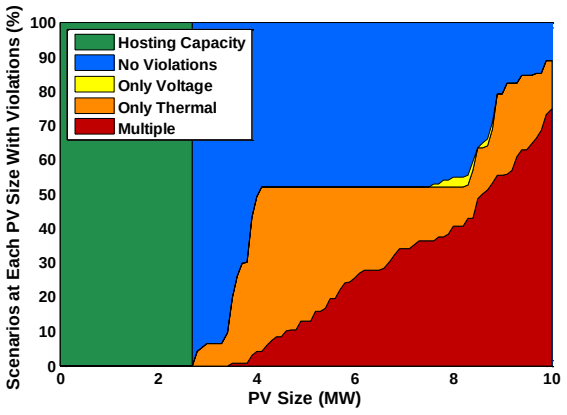




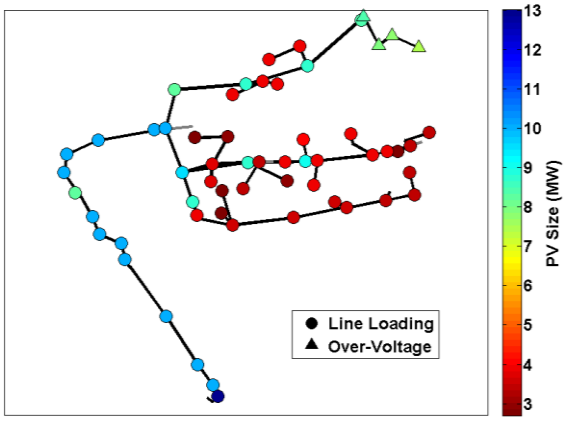
Bottom of Band bus voltages average 3.01 V lower

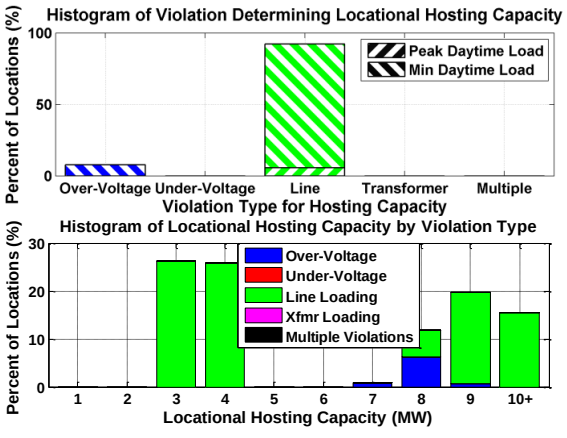
PV Impact Signature



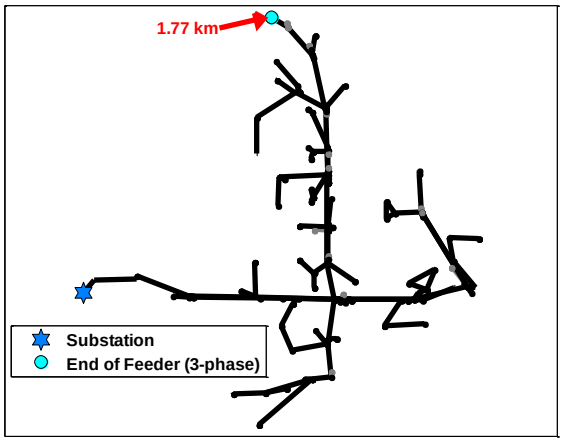


Locational Hosting Capacity

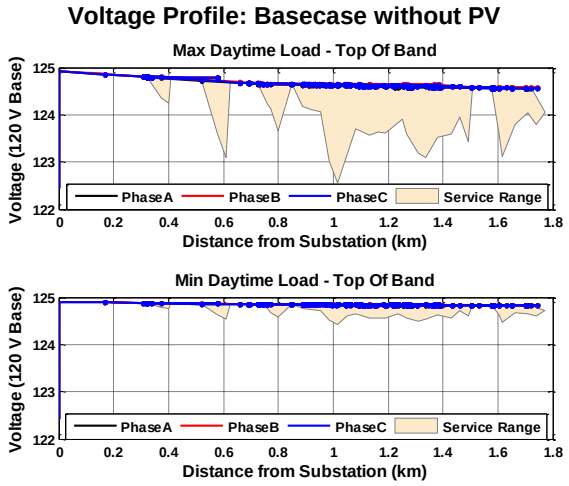




DK1

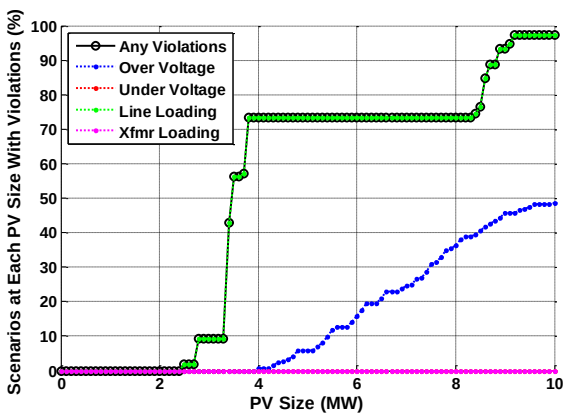


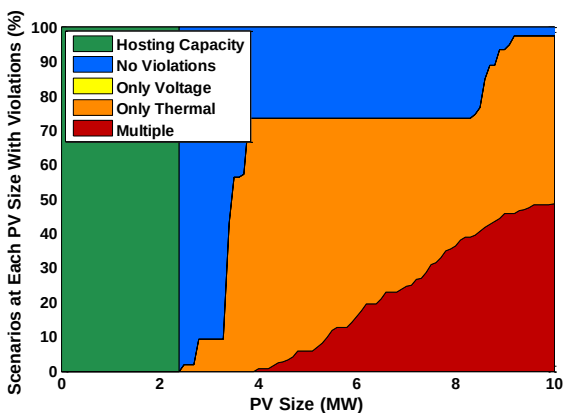
12 kV, 3.59 MW peak load
Max daytime load = 3.59 MW (100%)
Min daytime load = 0.74 MW (20%)



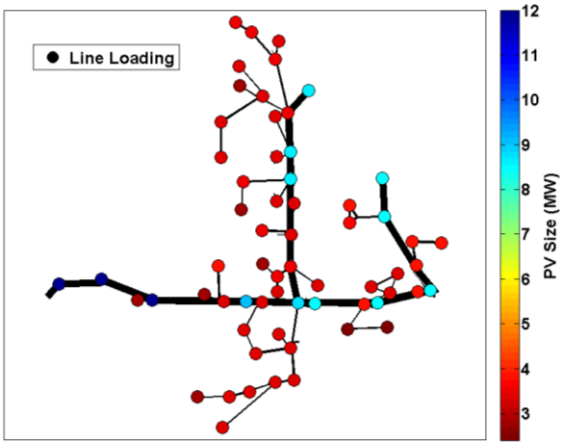
Bottom of Band bus voltages average 3.97 V lower

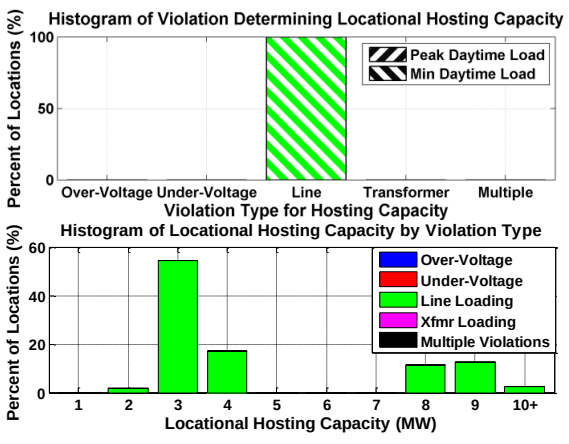
PV Impact Signature



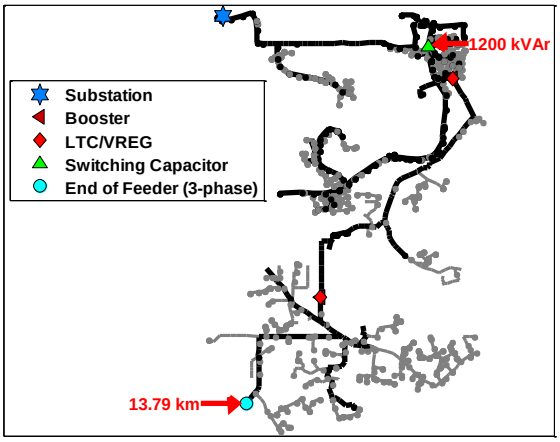


Locational Hosting Capacity

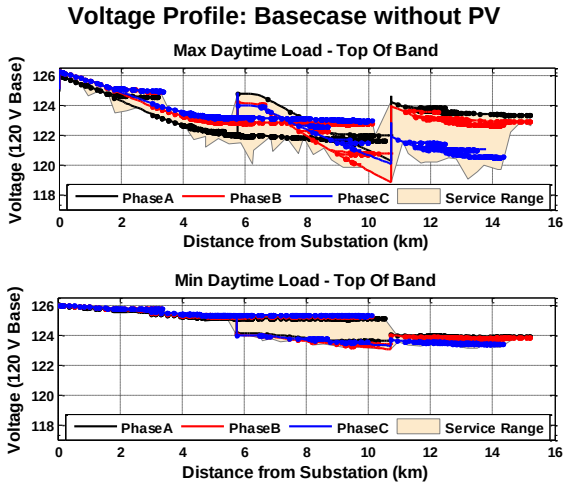




DS1

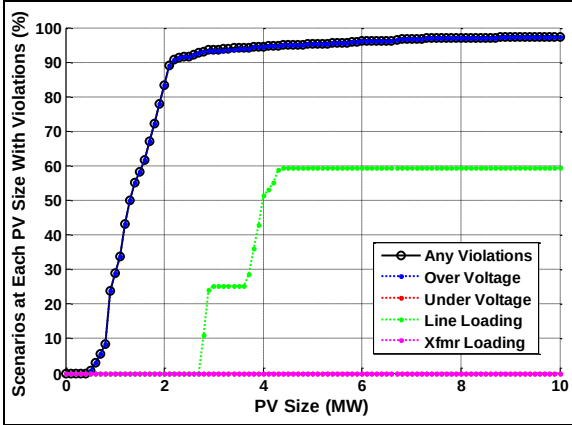


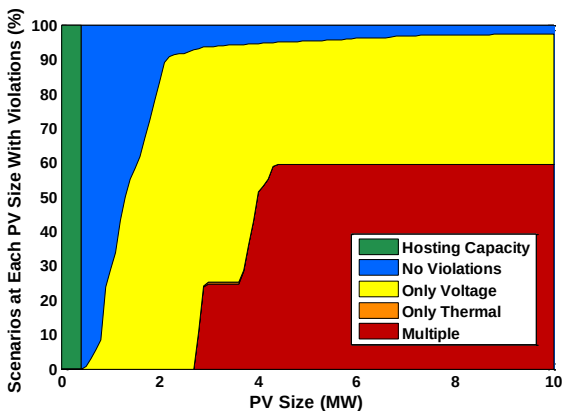
12 kV, 10.20 MW peak load
Max daytime load = 8.13 MW (80%)
Min daytime load = 1.49 MW (15%)



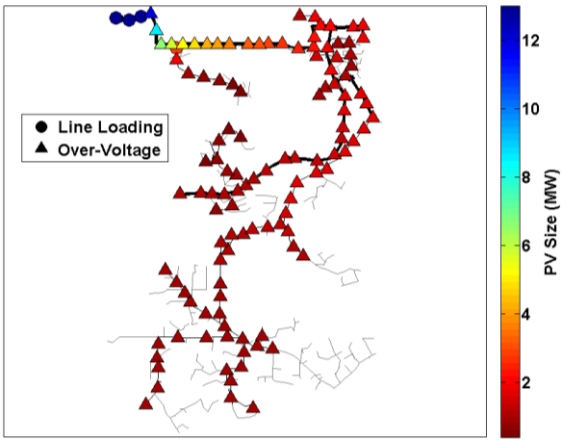
Bottom of Band bus voltages average 2.21 V lower

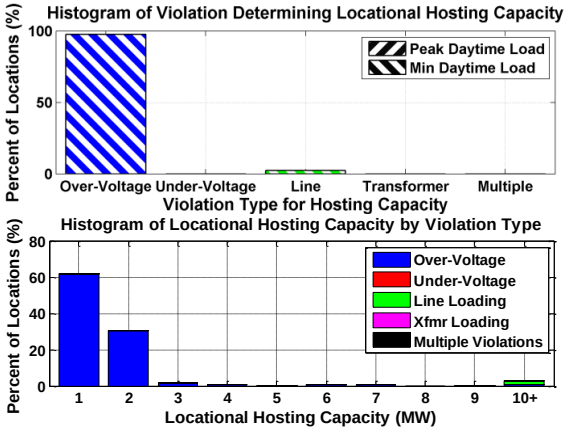
PV Impact Signature



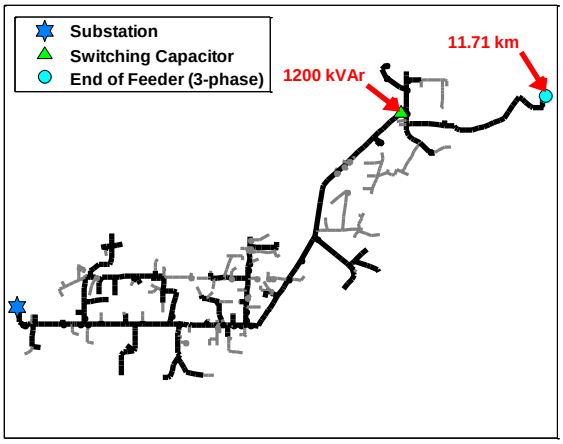


Locational Hosting Capacity

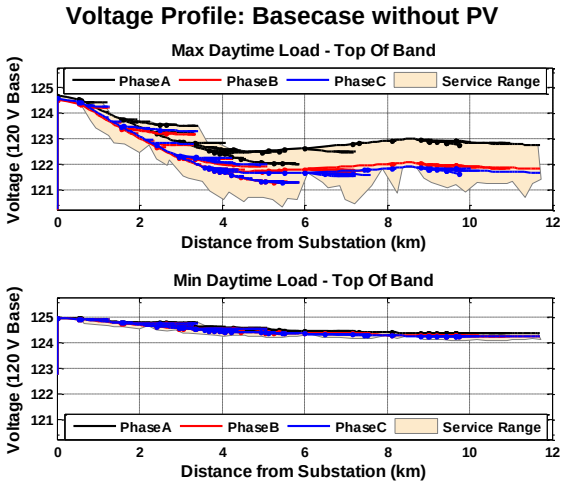




DV1

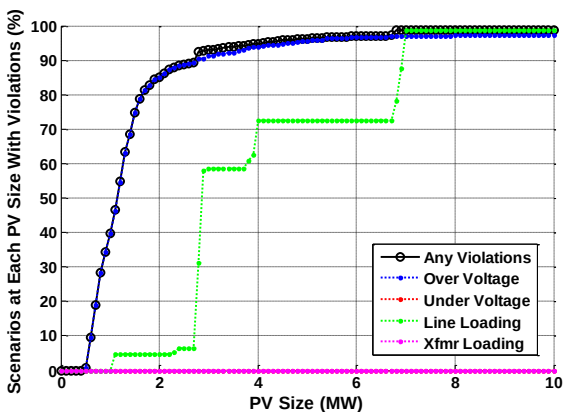


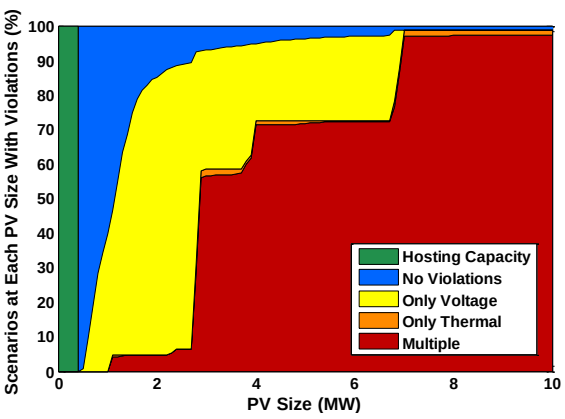
12 kV, 3.42 MW peak load
Max daytime load = 3.39 MW (99%)
Min daytime load = 0.42 MW (12%)



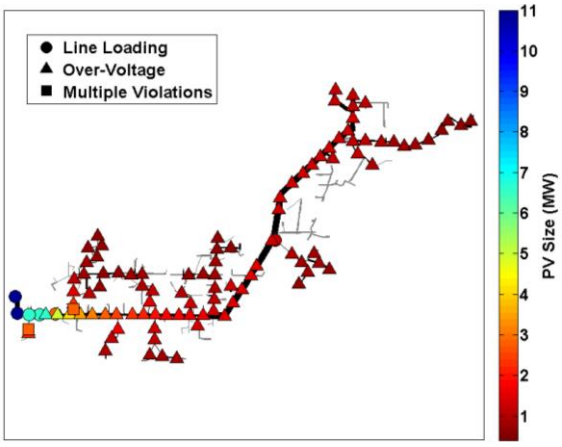
Bottom of Band bus voltages average 3.93 V lower

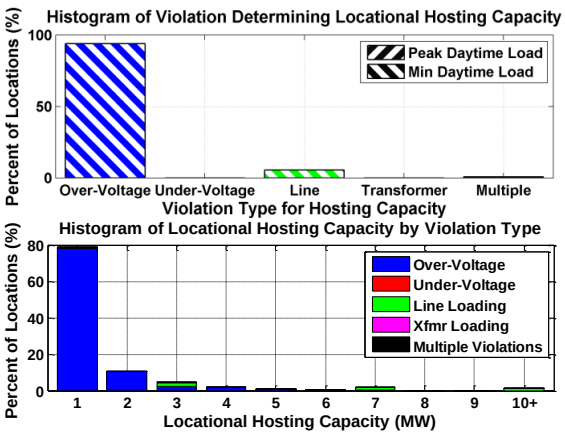
PV Impact Signature



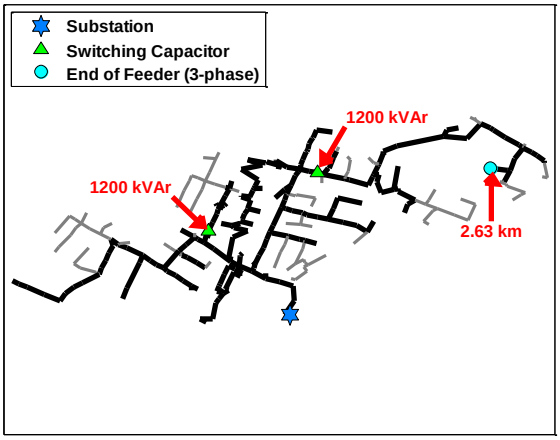


Locational Hosting Capacity



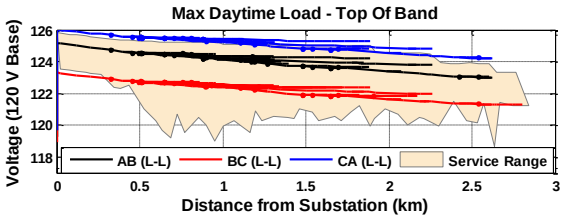


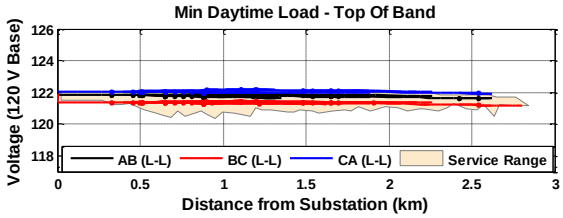
QL2



12 kV, 5.16 MW peak load
Max daytime load = 5.07 MW (98%)
Min daytime load = 1.37 MW (26%)

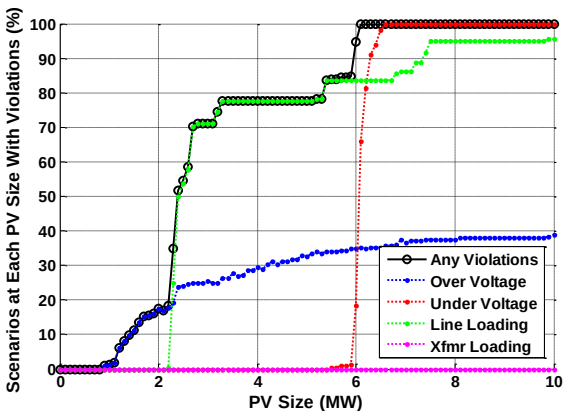
Voltage Profile: Basecase without PV

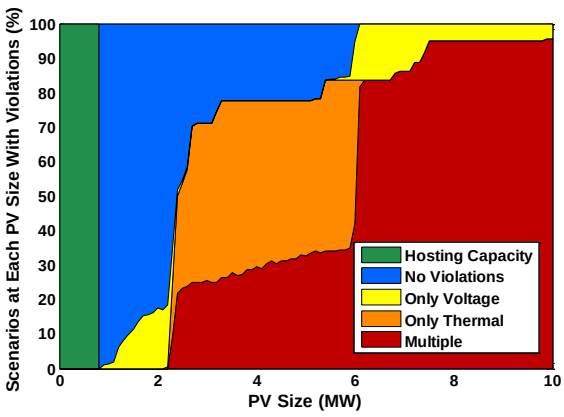




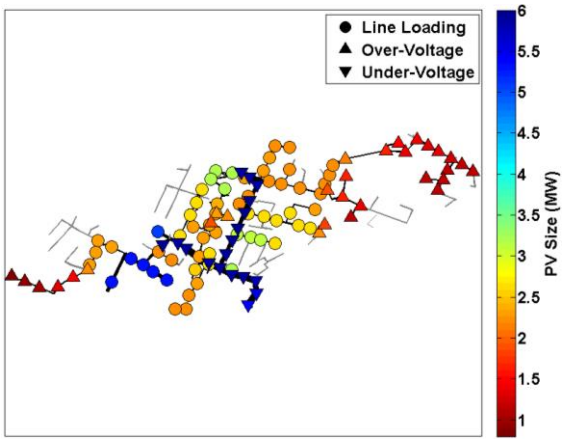
Bottom of Band bus voltages average 1.99 V lower

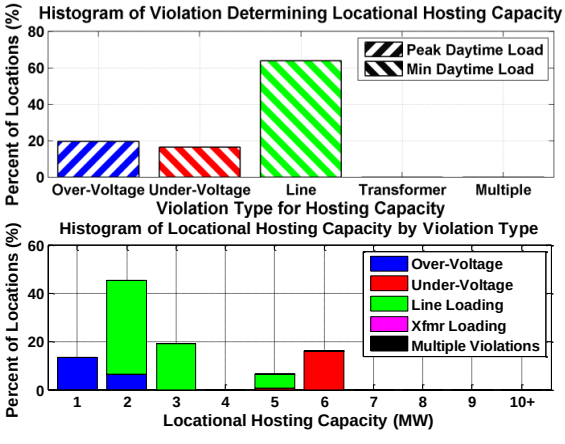
PV Impact Signature



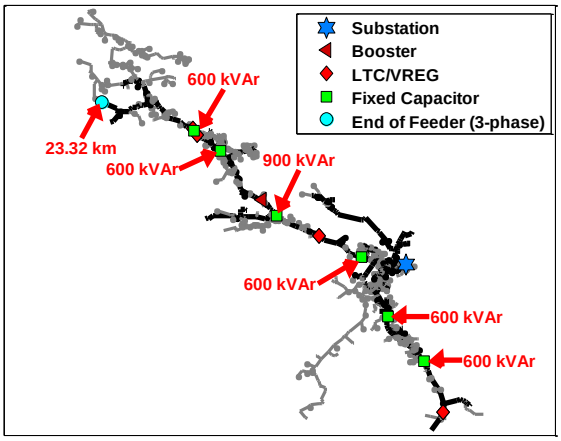


Locational Hosting Capacity



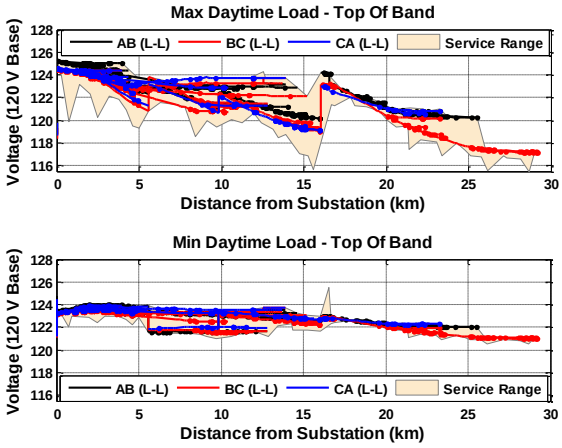


QM1



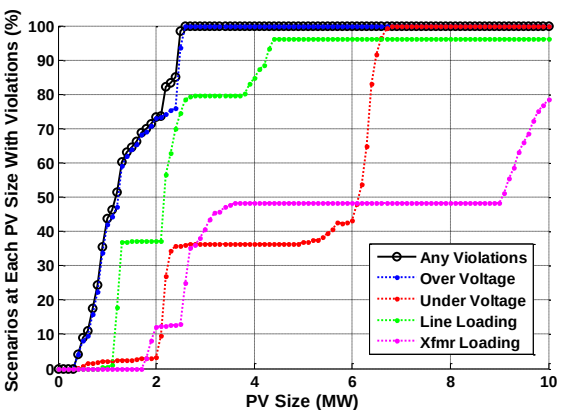
12 kV, 6.10 MW peak load
Max daytime load = 5.87 MW (96%)
Min daytime load = 1.92 MW (29%)

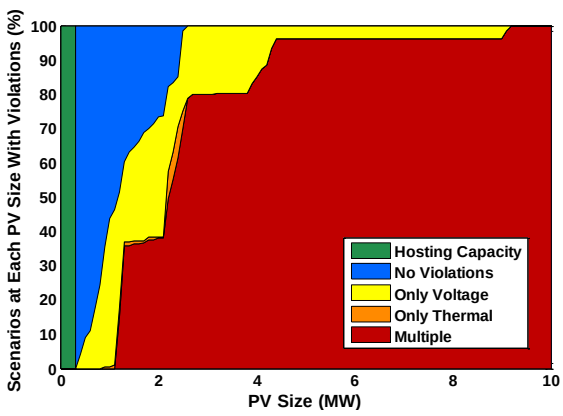
Voltage Profile: Basecase without PV



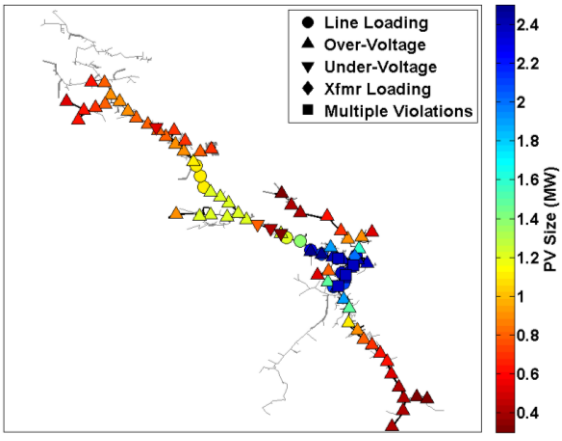
Bottom of Band bus voltages average 1.81 V lower

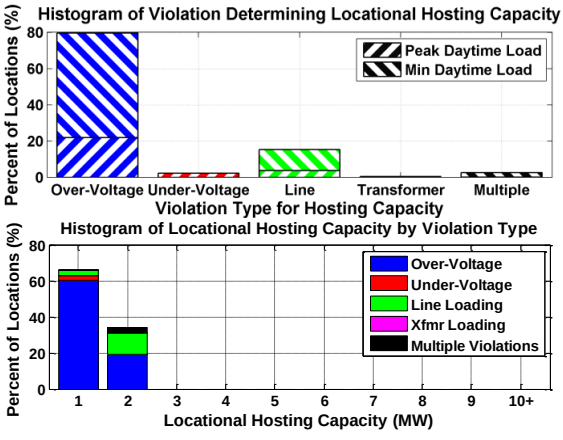
PV Impact Signature



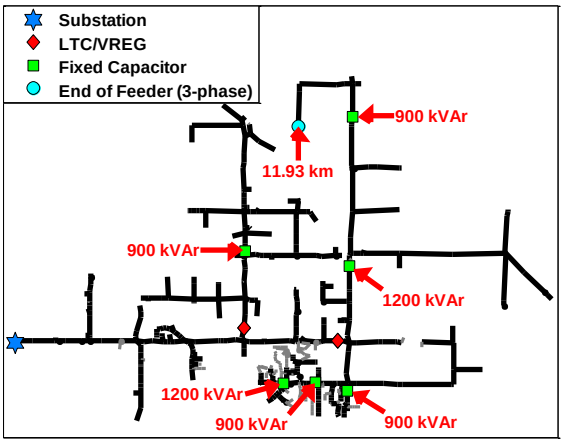


Locational Hosting Capacity



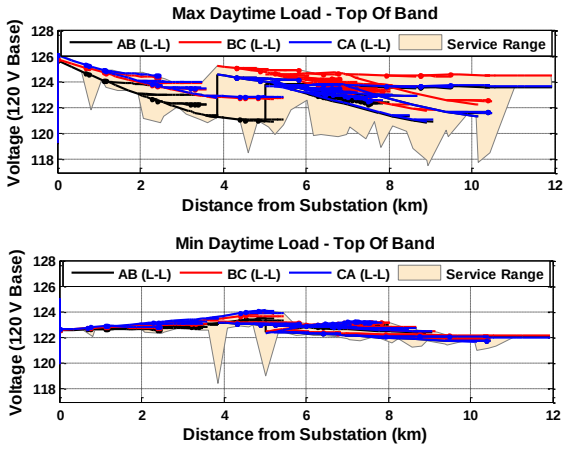


QS1



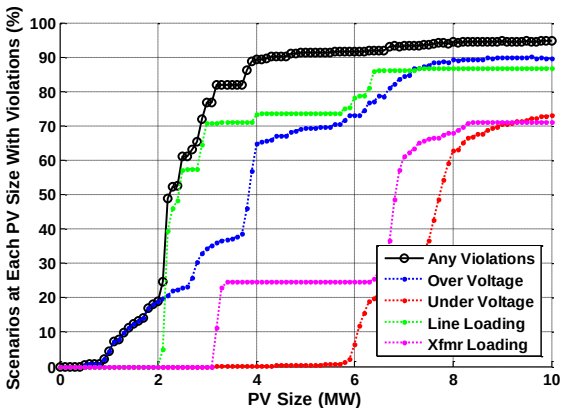
12 kV, 9.25 MW peak load
Max daytime load = 8.92 MW (97%)
Min daytime load = 1.96 MW (19%)

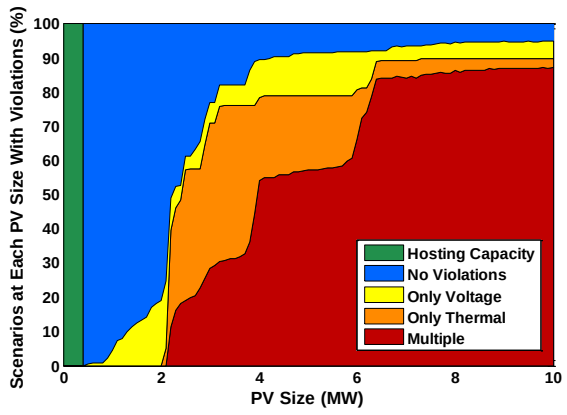
Voltage Profile: Basecase without PV



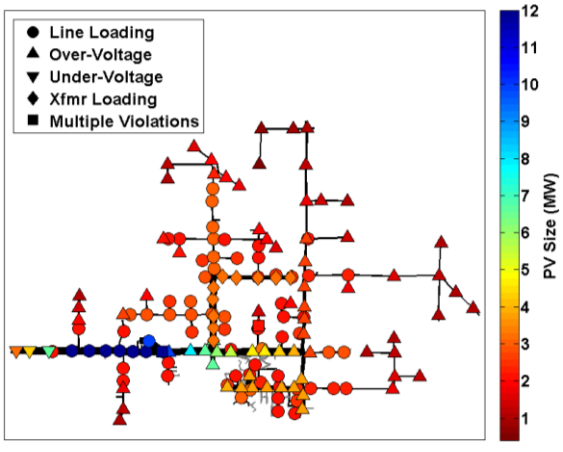
Bottom of Band bus voltages average 1.69 V lower

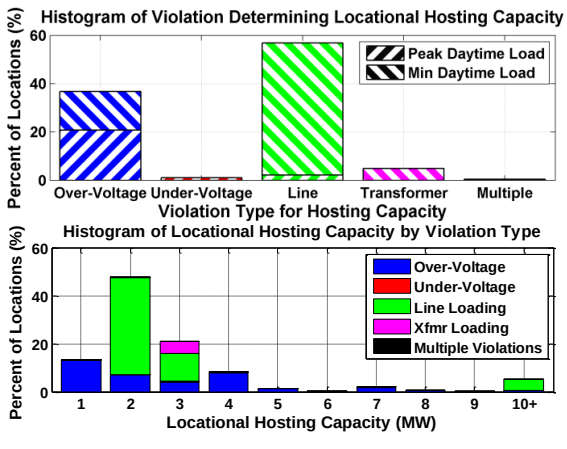
PV Impact Signature



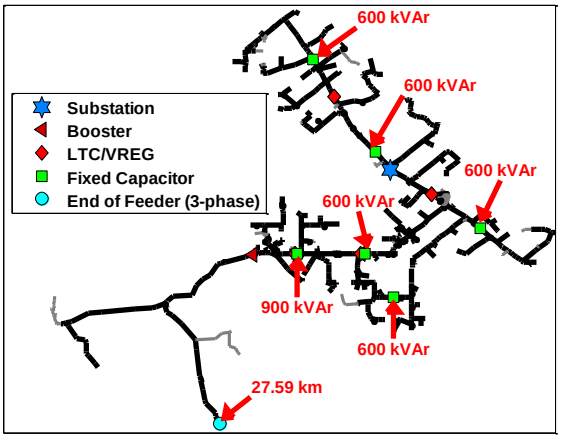


Locational Hosting Capacity

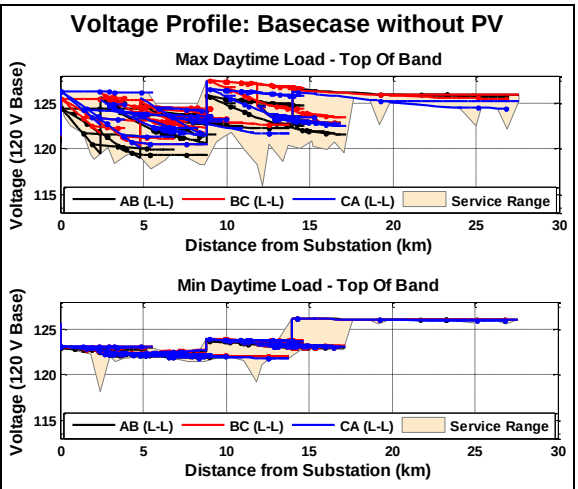




QW1

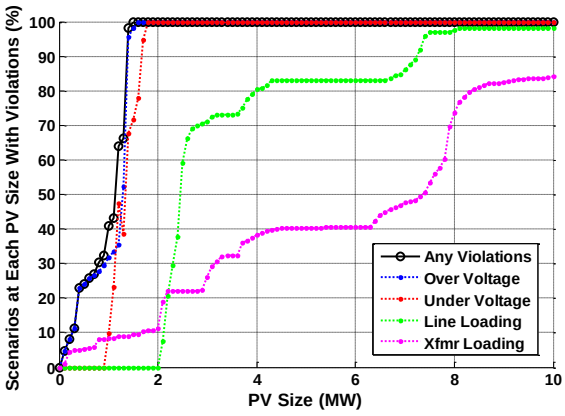


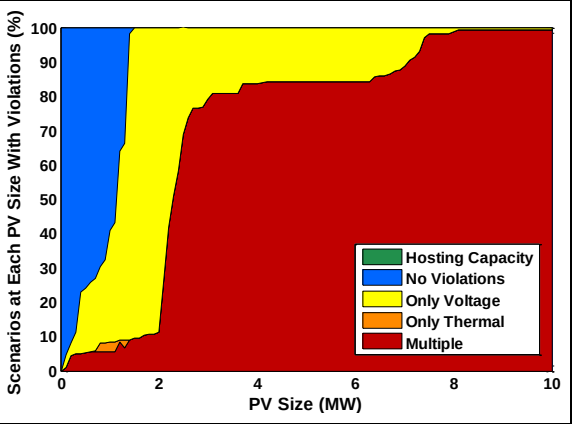
12 kV, 8.44 MW peak load
Max daytime load = 8.29 MW (98%)
Min daytime load = 1.13 MW (13%)



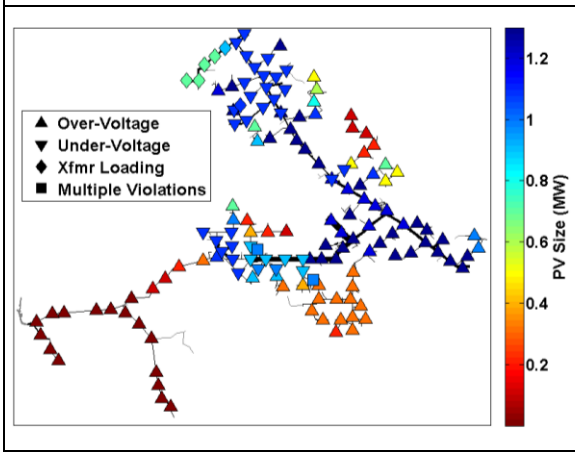
Bottom of Band bus voltages average 1.83 V lower

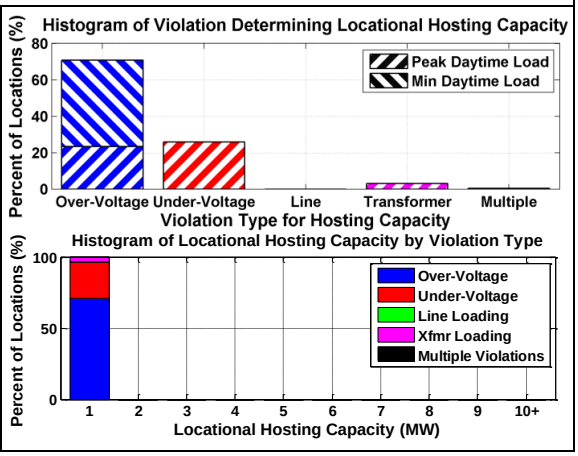
PV Impact Signature



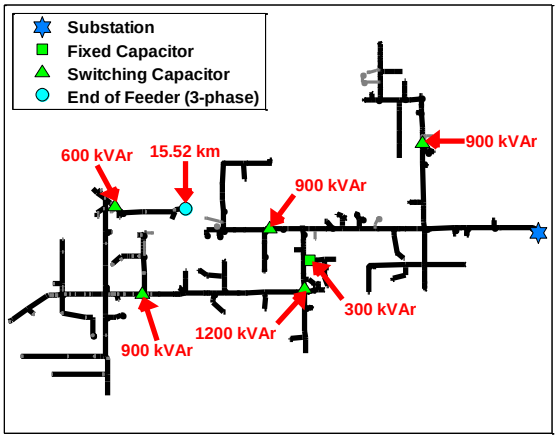


Locational Hosting Capacity

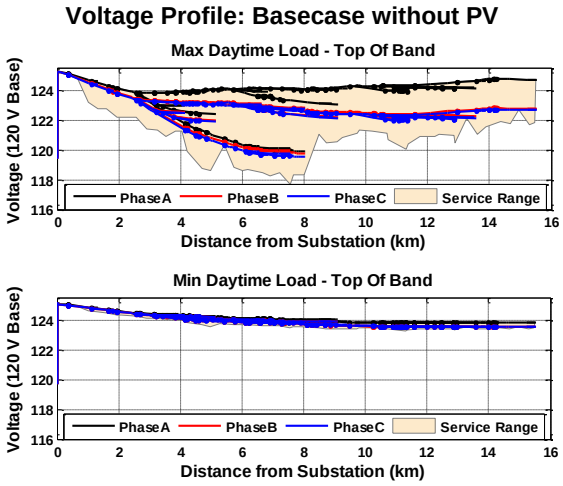




CG1

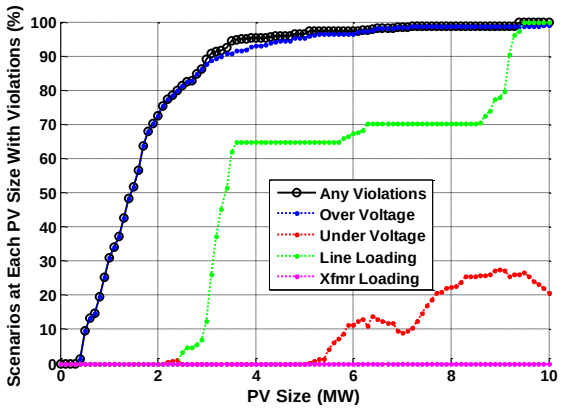


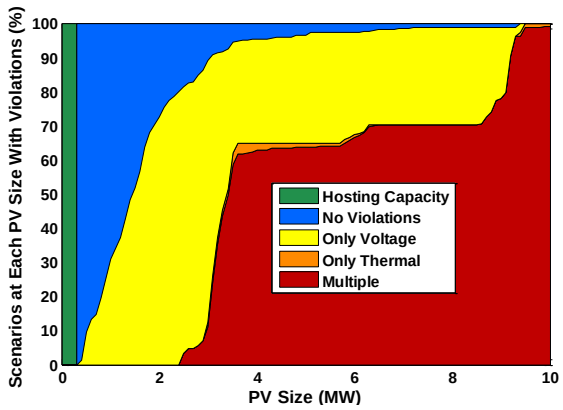
12 kV, 6.35 MW peak load
Max daytime load = 6.29 MW (99%)
Min daytime load = 0.85 MW (13%)



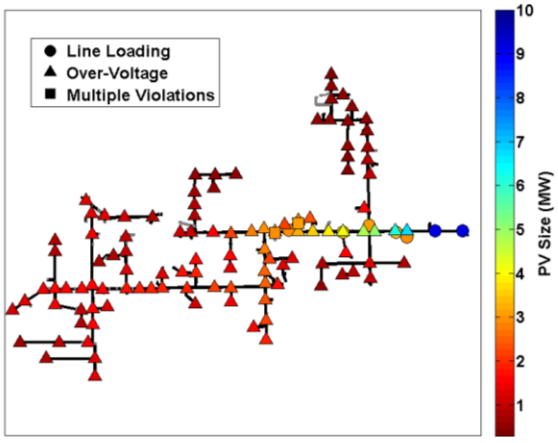
Bottom of Band bus voltages average 2.34 V lower

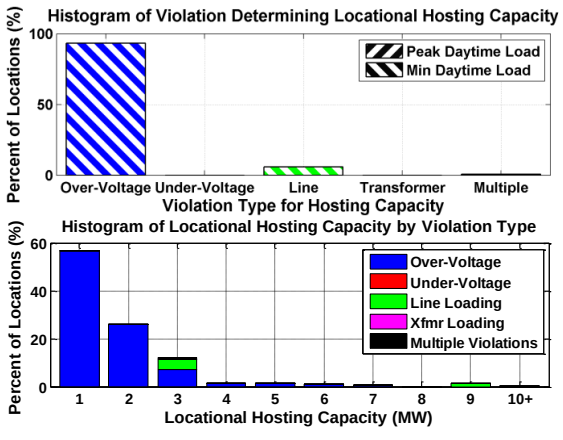
PV Impact Signature



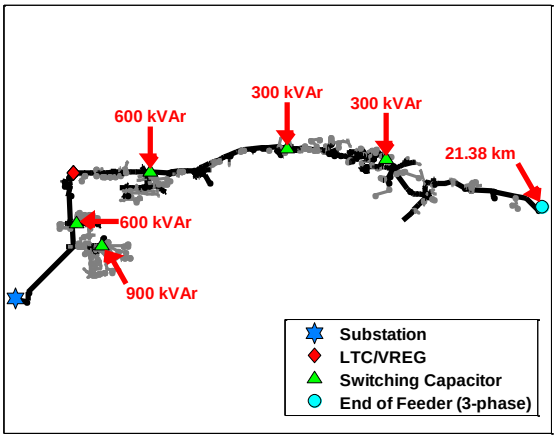


Locational Hosting Capacity

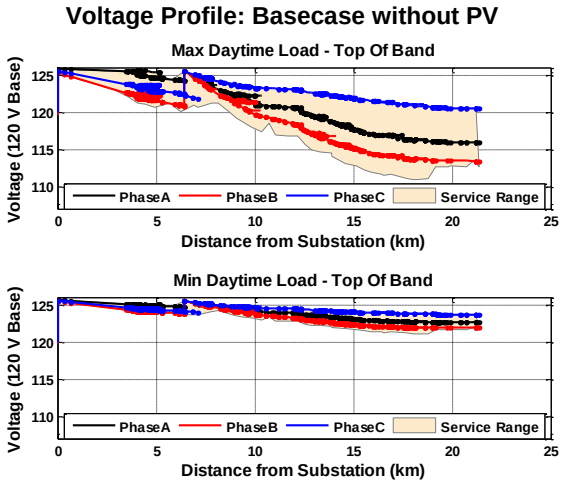




CO1

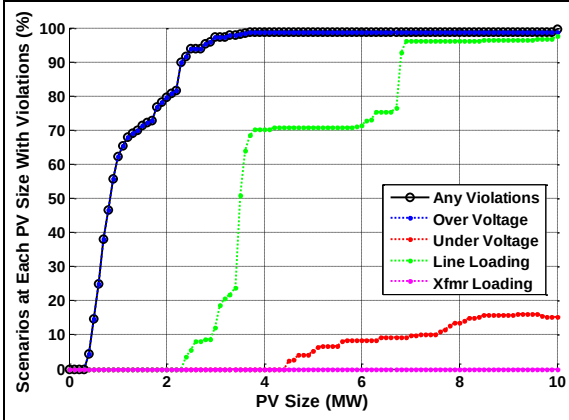


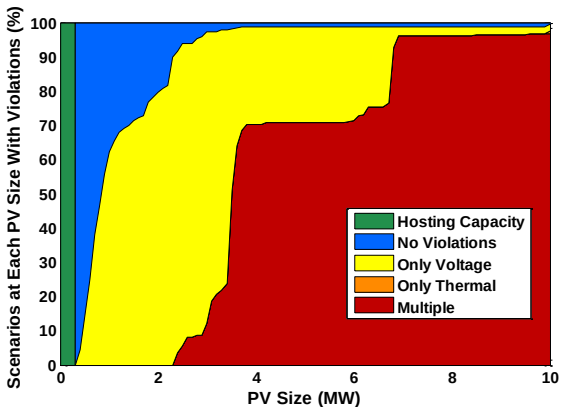
12 kV, 6.39 MW peak load
Max daytime load = 5.79 MW (91%)
Min daytime load = 1.52 MW (24%)



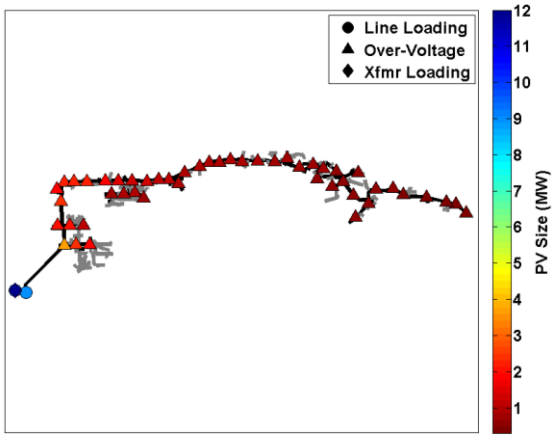
Bottom of Band bus voltages average 1.12 V lower

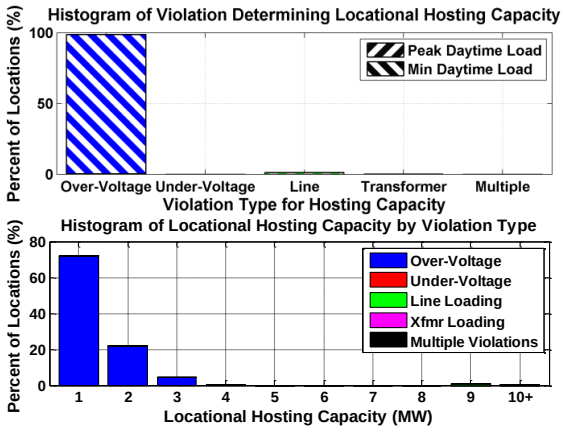
PV Impact Signature



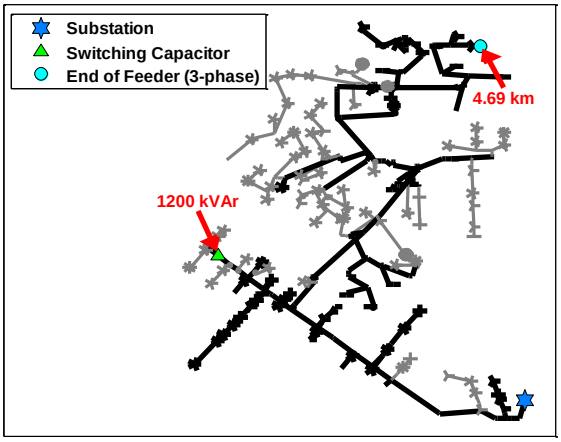


Locational Hosting Capacity



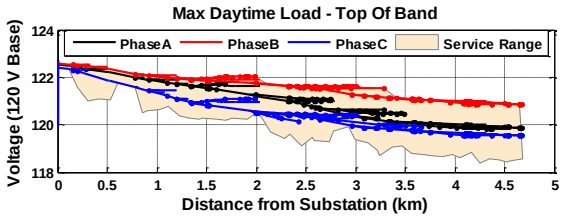


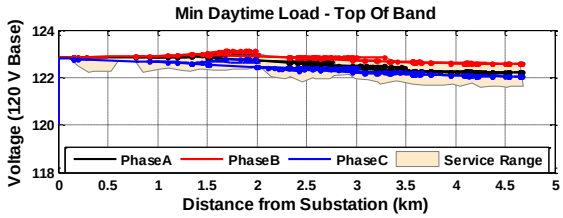
CS1



12 kV, 5.00 MW peak load
Max daytime load = 4.92 MW (98%)
Min daytime load = 1.95 MW (39%)

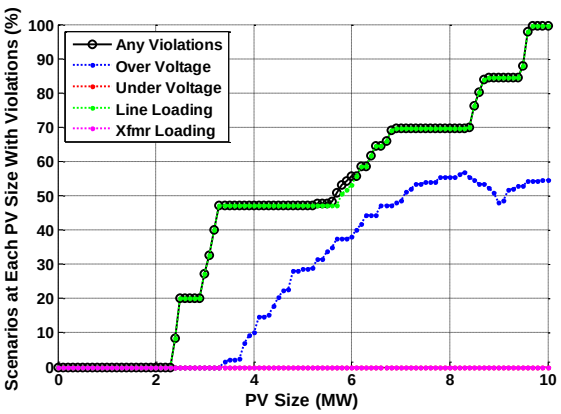
Voltage Profile: Basecase without PV

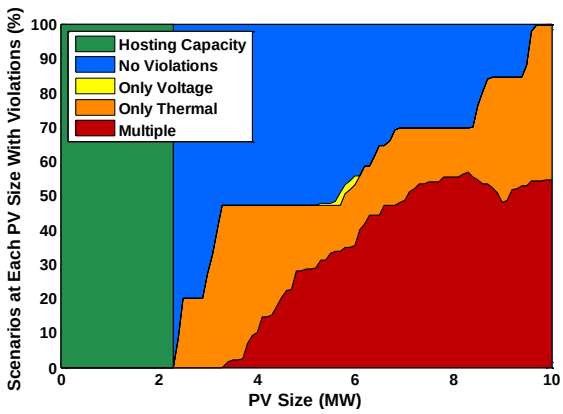




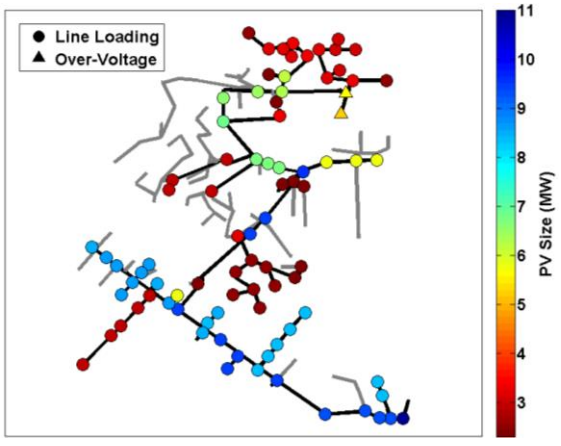
Bottom of Band bus voltages average 1.17 V lower

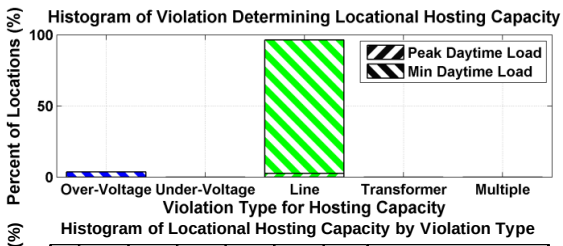
PV Impact Signature

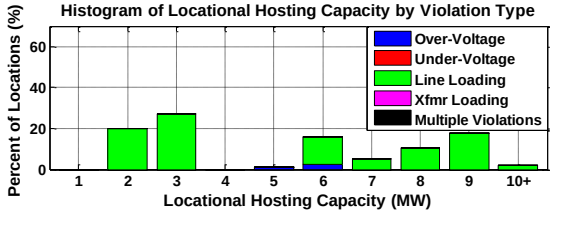




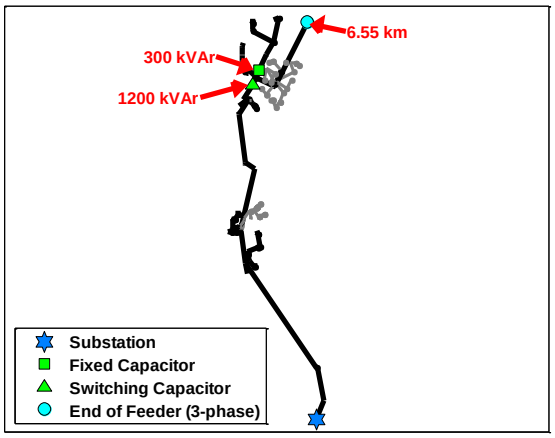
Locational Hosting Capacity





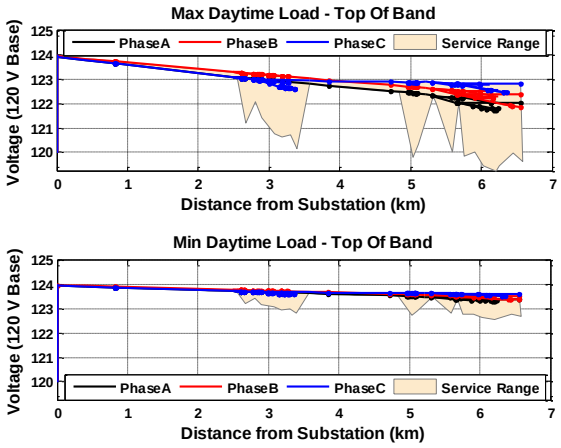


CV1



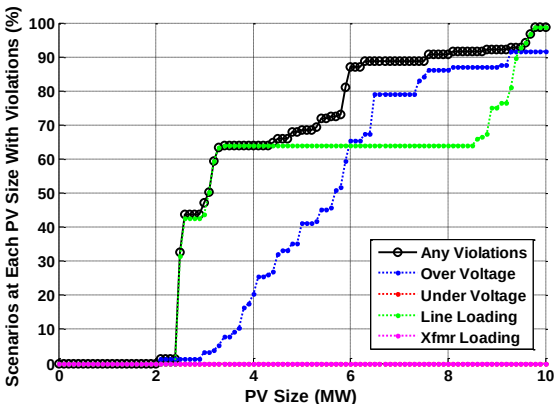
12 kV, 4.29 MW peak load
Max daytime load = 4.00 MW (93%)
Min daytime load = 1.13 MW (26%)

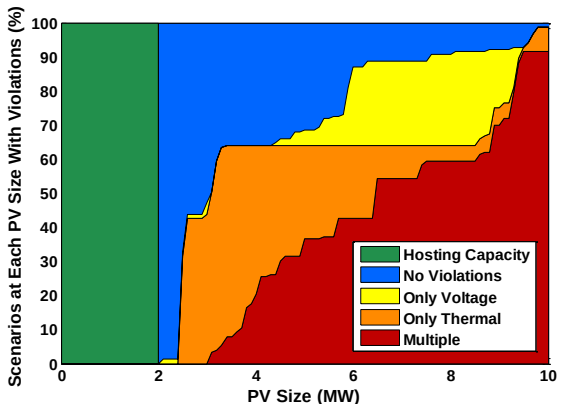
Voltage Profile: Basecase without PV



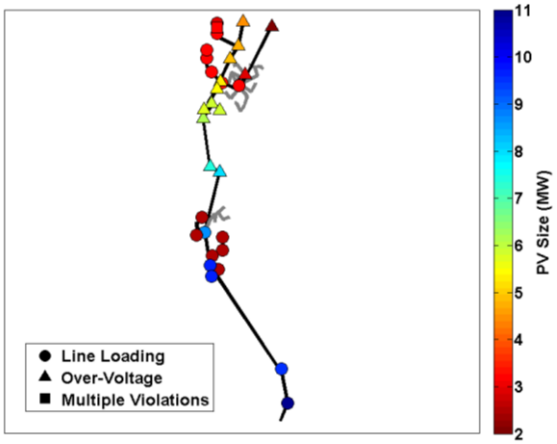
Bottom of Band bus voltages average 1.36 V lower

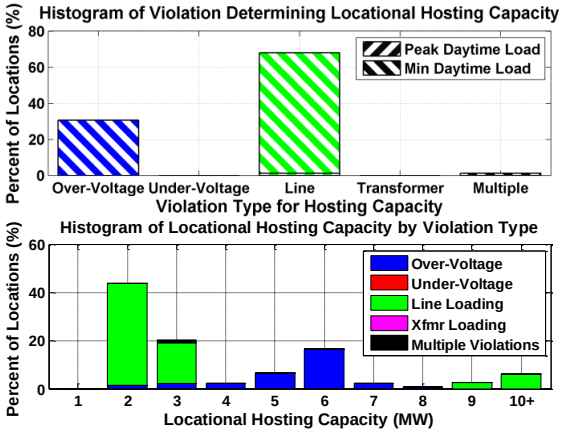
PV Impact Signature



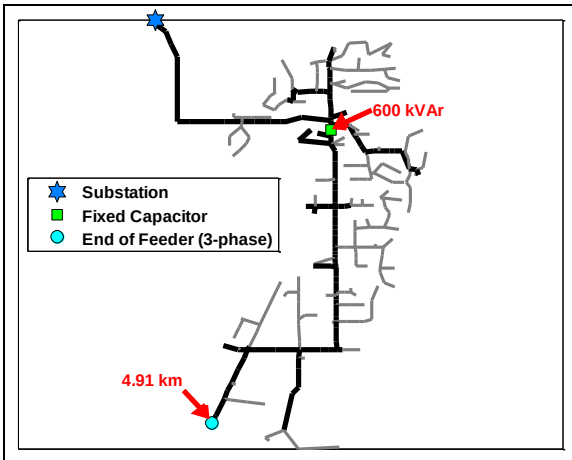


Locational Hosting Capacity

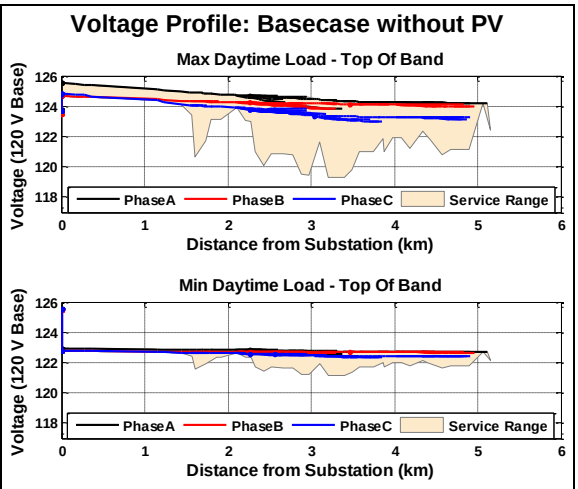




UQ11

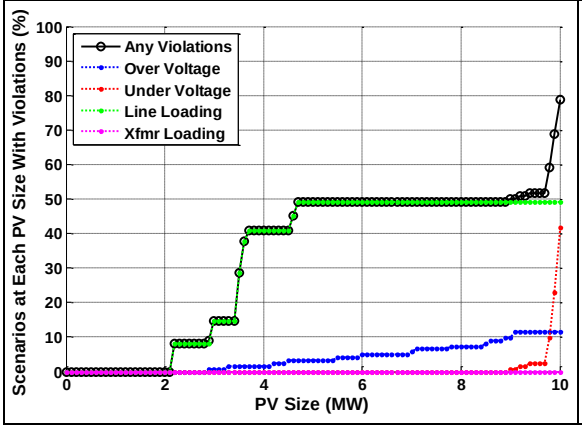


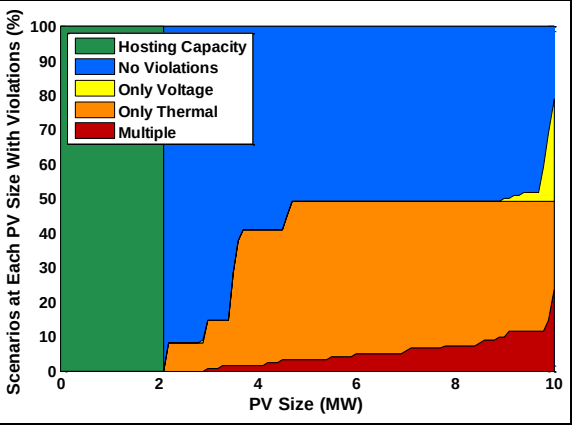
12.47 kV, 3.43 MW peak load
Max daytime load = 3.20 MW (93%)
Min daytime load = 1.01 MW (28%)



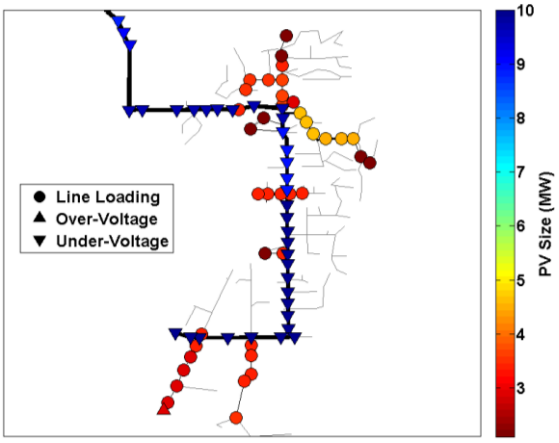
Bottom of Band bus voltages average 1.90V lower

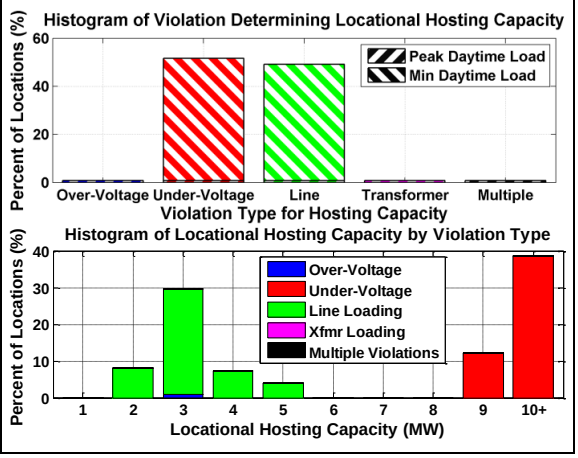
PV Impact Signature



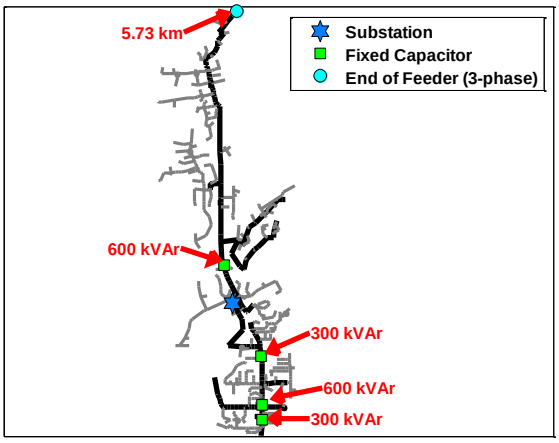


Locational Hosting Capacity

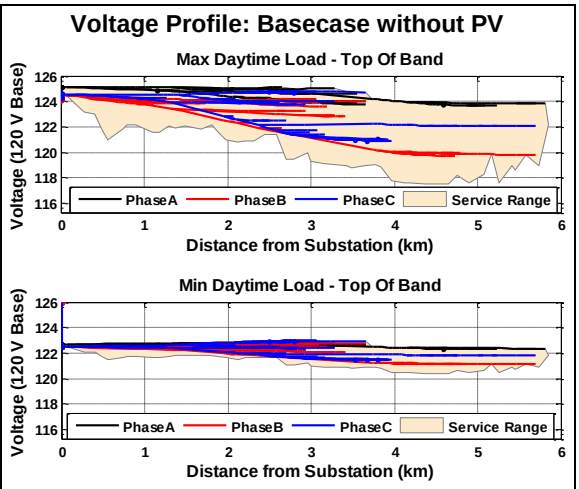




UQ12

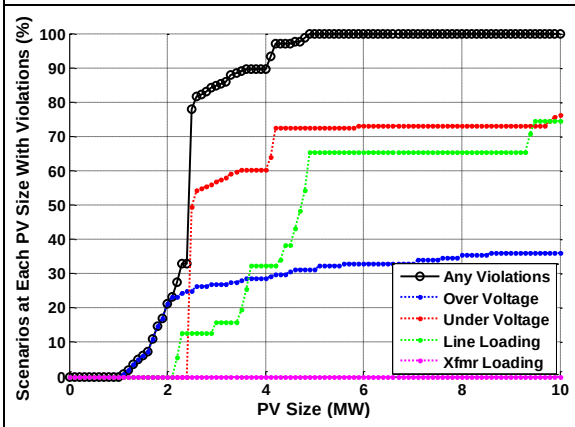


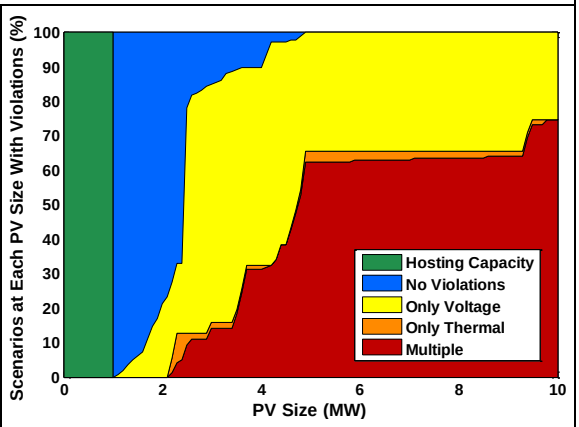
12.47 kV, 6.19 MW peak load
Max daytime load = 5.43 MW (87%)
Min daytime load = 1.75 MW (27%)



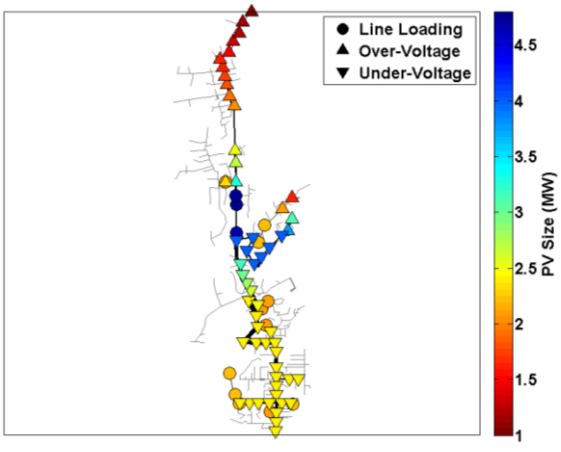
Bottom of Band bus voltages average 1.92V lower

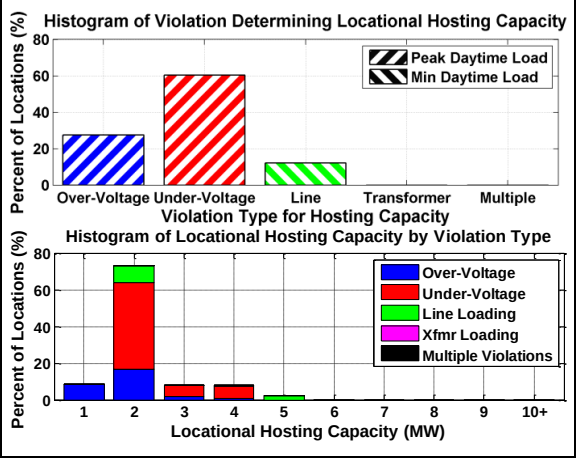
PV Impact Signature



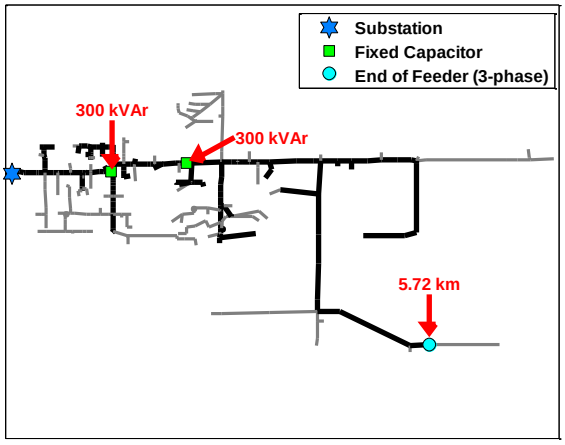


Locational Hosting Capacity

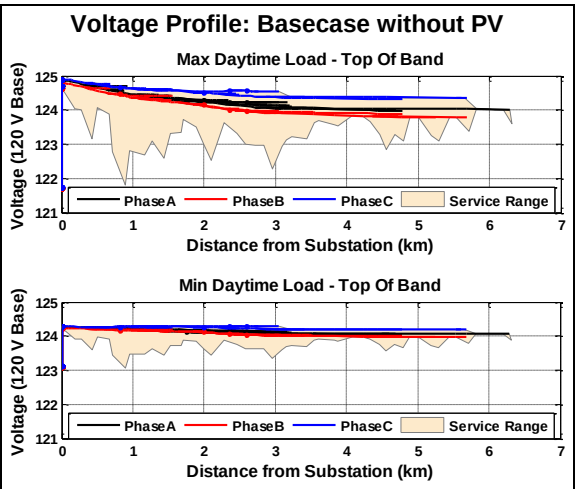




UD11

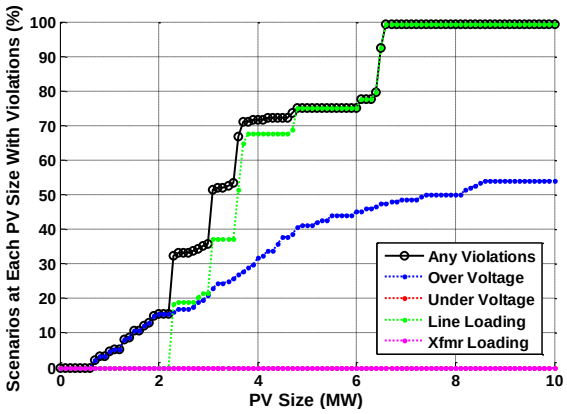


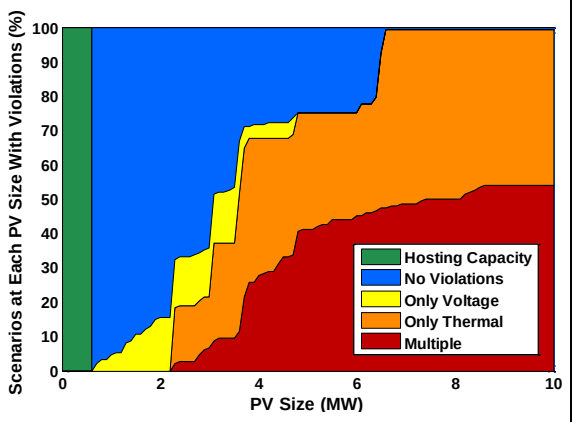
12.47 kV, 1.71 MW peak load
Max daytime load = 1.63 MW (96%)
Min daytime load = 0.73 MW (40%)



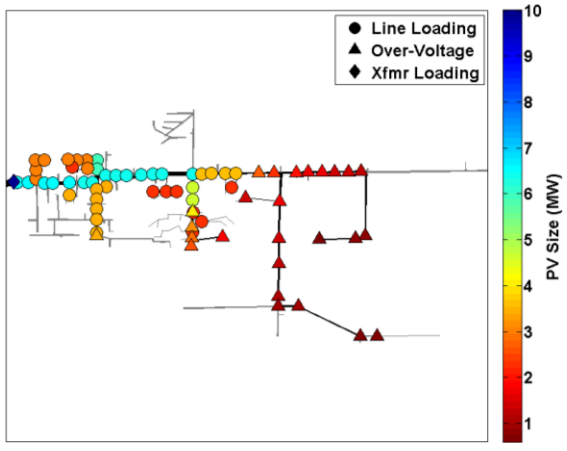
Bottom of Band bus voltages average 1.85V lower

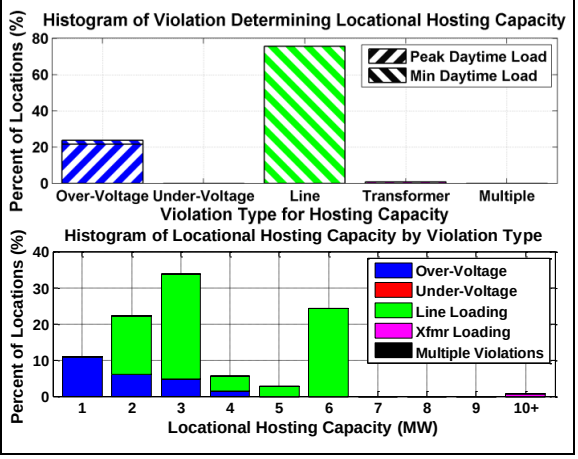
PV Impact Signature



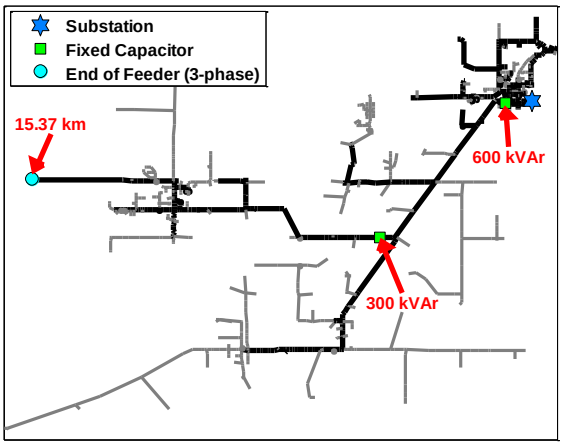


Locational Hosting Capacity

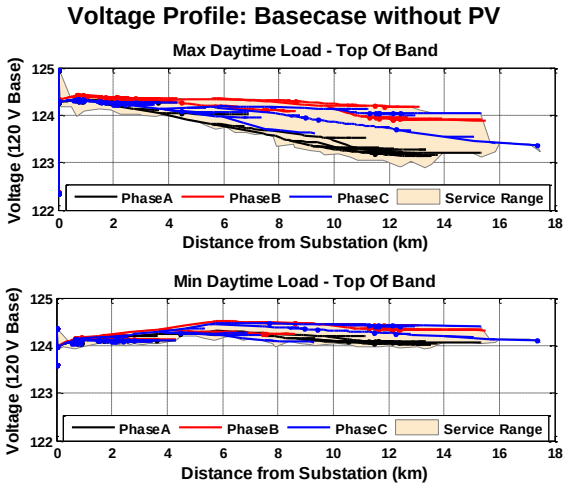




UD12

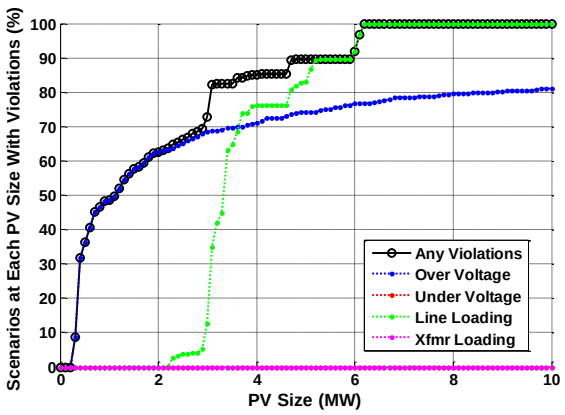


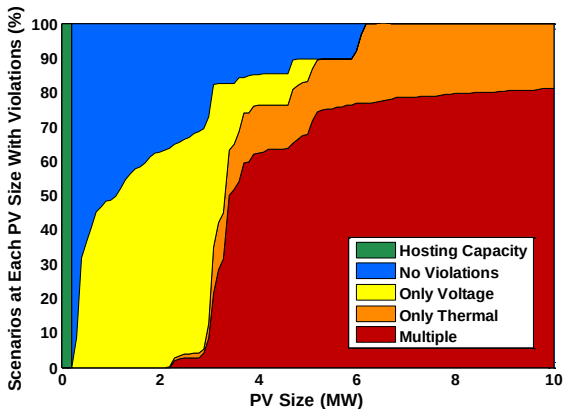
12.47 kV, 0.72 MW peak load
Max daytime load = 0.68 MW (92%)
Min daytime load = 0.37 MW (34%)



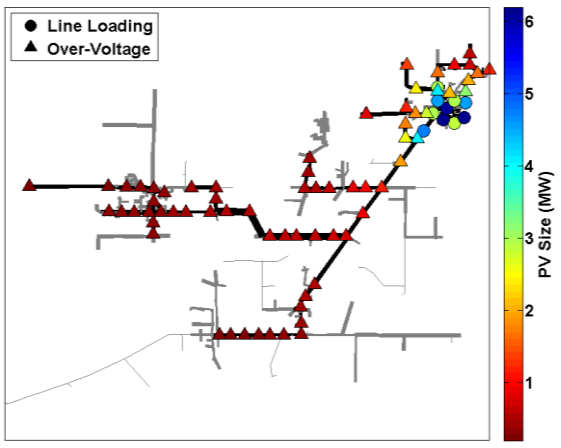
Bottom of Band bus voltages average 1.93V lower

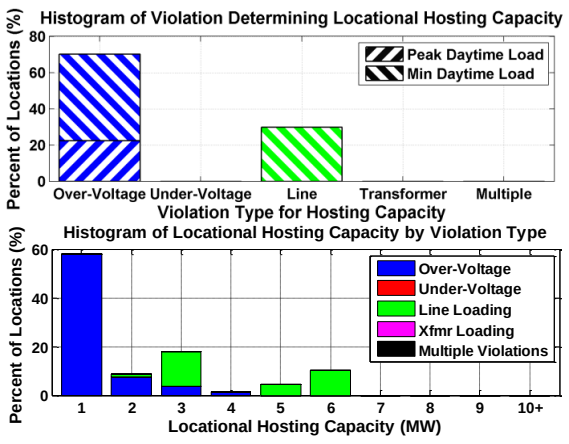
PV Impact Signature



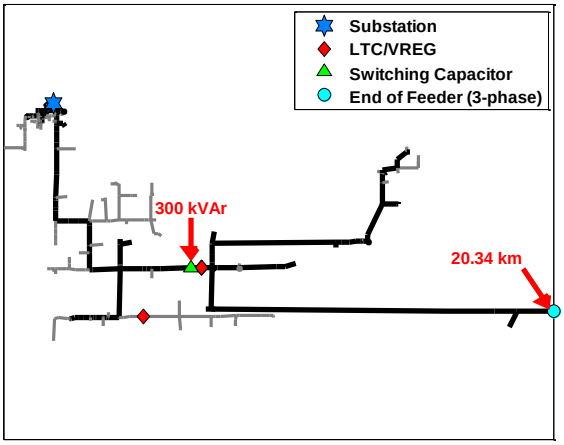


Locational Hosting Capacity

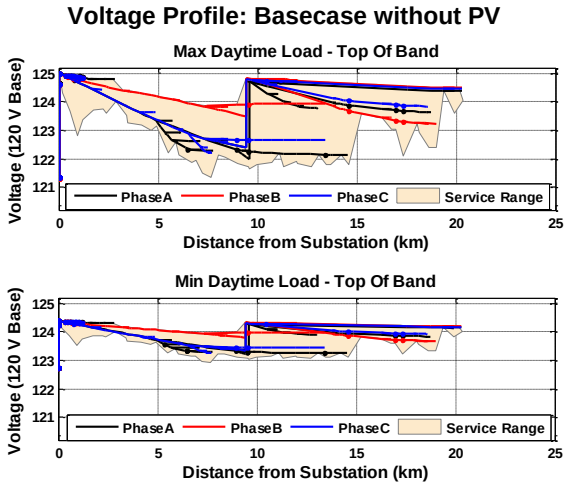




UD13

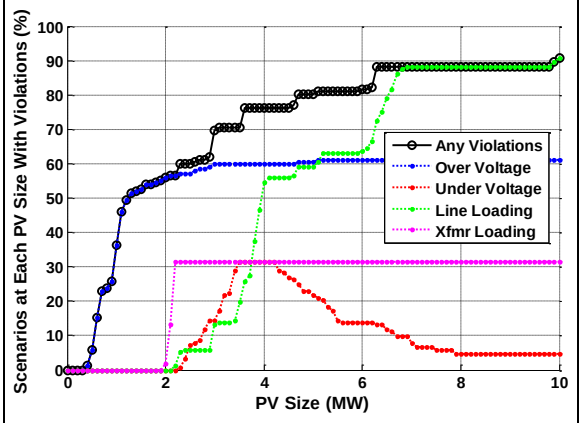


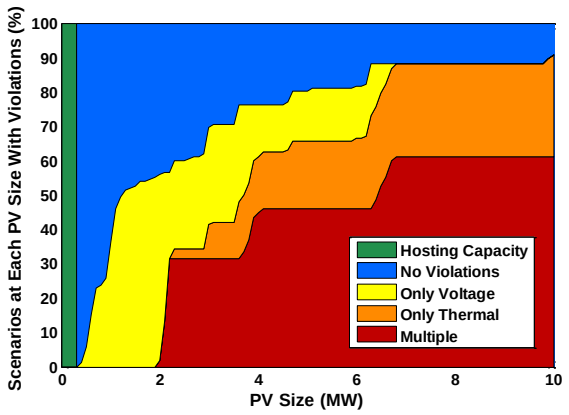
12.47 kV, 1.17 MW peak load
Max daytime load = 1.15 MW (98%)
Min daytime load = 0.50 MW (39%)



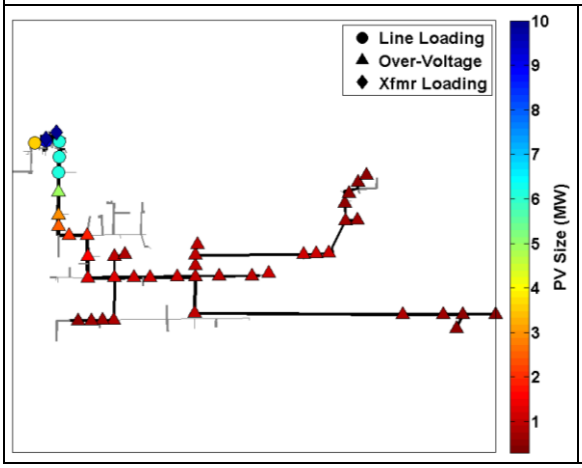
Bottom of Band bus voltages average 1.86V lower

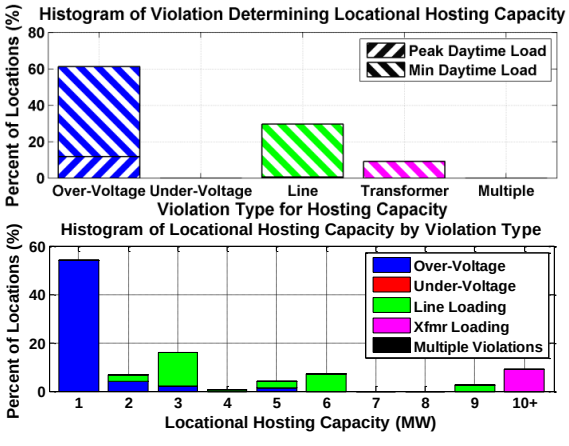
PV Impact Signature



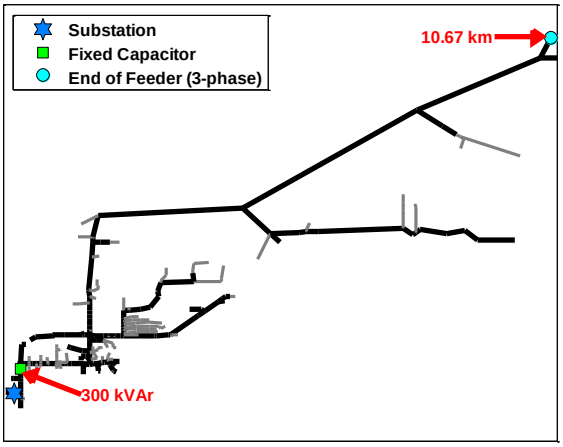


Locational Hosting Capacity

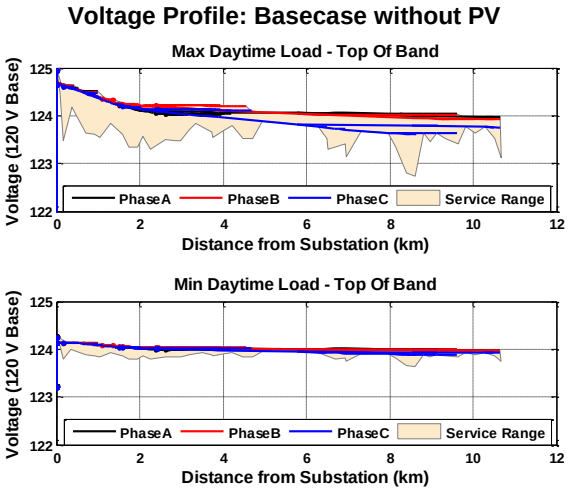




UD14

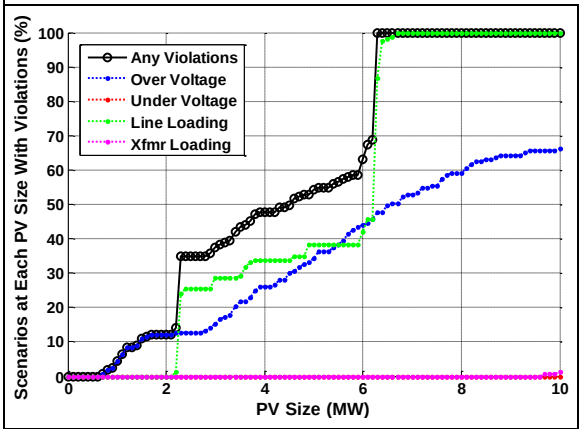


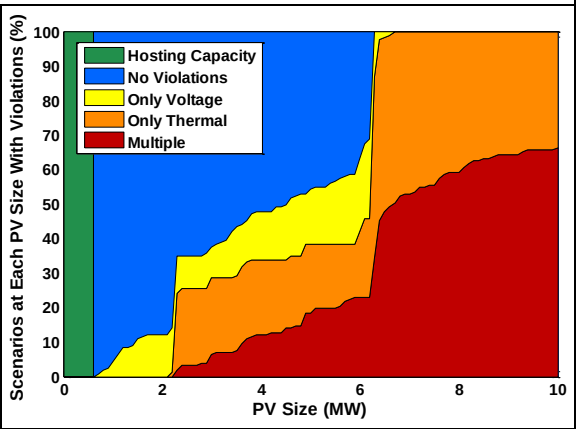
12.47 kV, 0.93 MW peak load
Max daytime load = 0.92 MW (99%)
Min daytime load = 0.32 MW (27%)



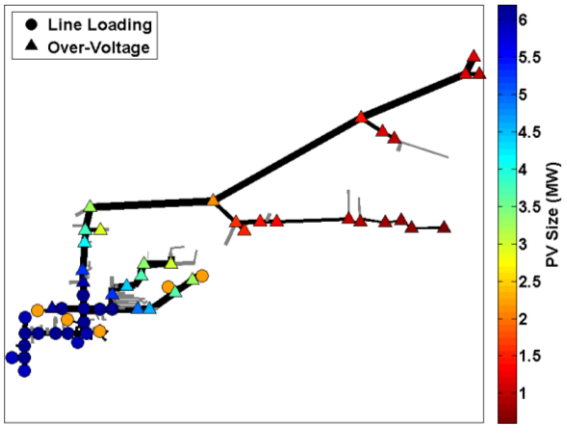
Bottom of Band bus voltages average 1.85V lower

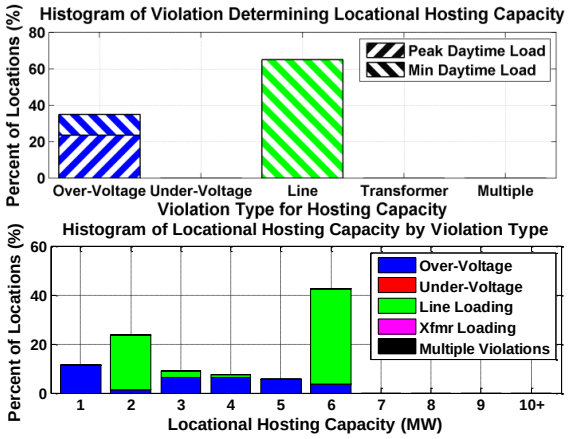
PV Impact Signature



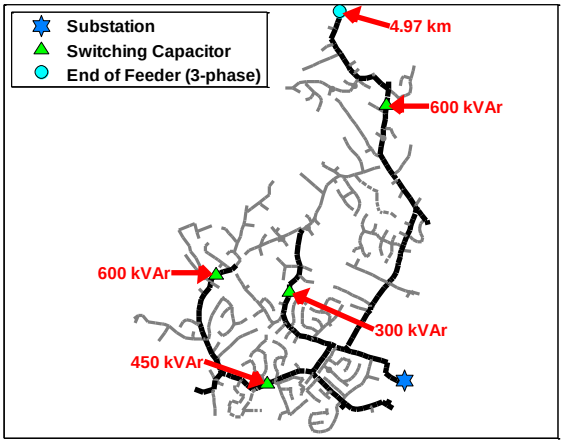


Locational Hosting Capacity

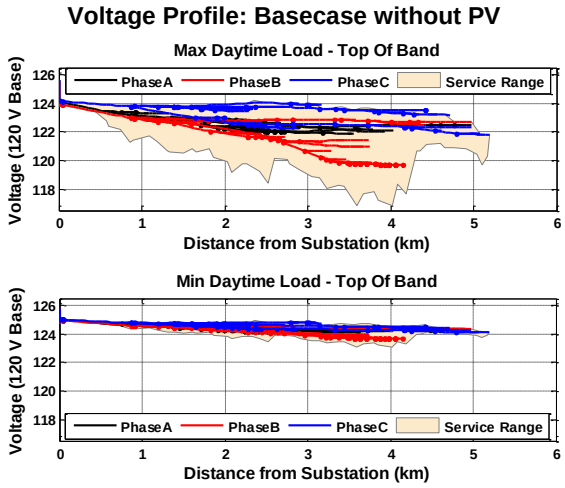




Ckt5

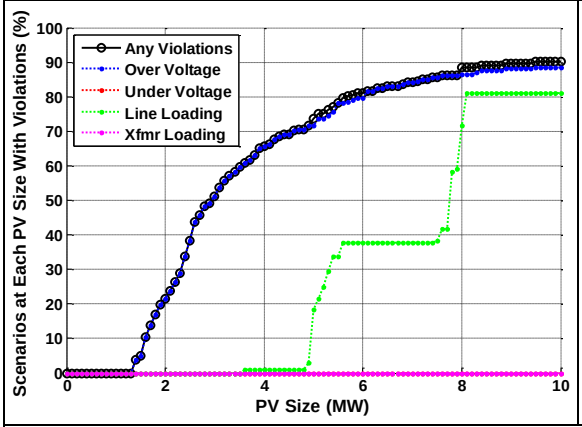


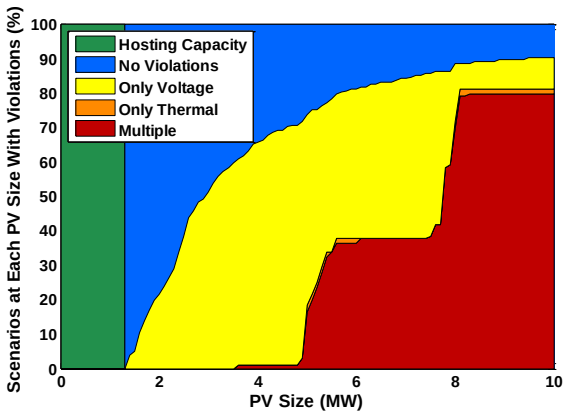
12.47 kV, 7.35 MW peak load
Max daytime load = 6.74 MW (91%)
Min daytime load = 1.74 MW (23%)



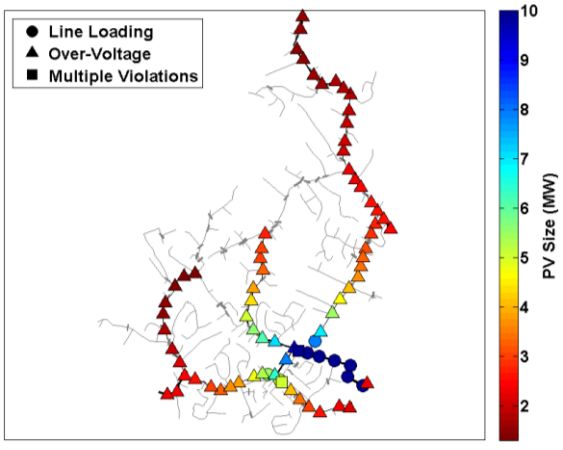
Bottom of Band bus voltages average 0.00V lower

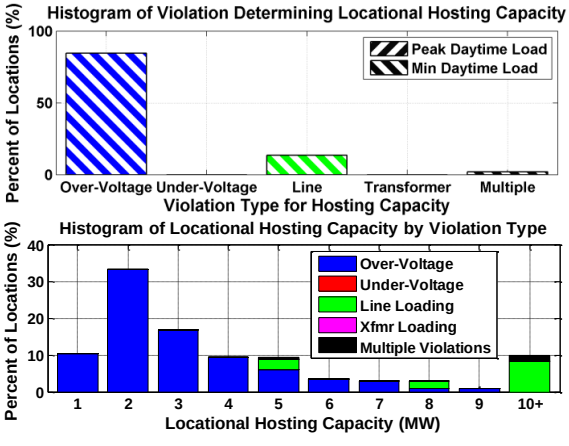
PV Impact Signature



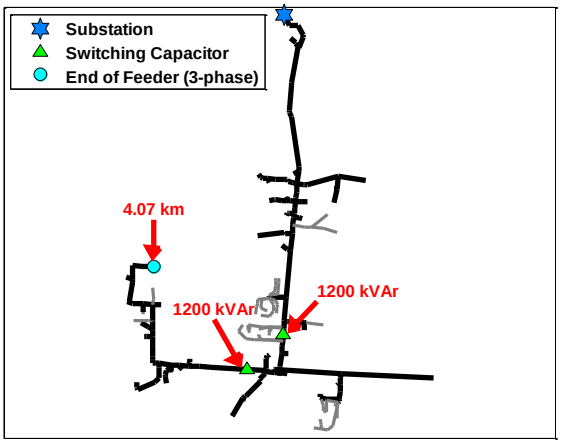


Locational Hosting Capacity

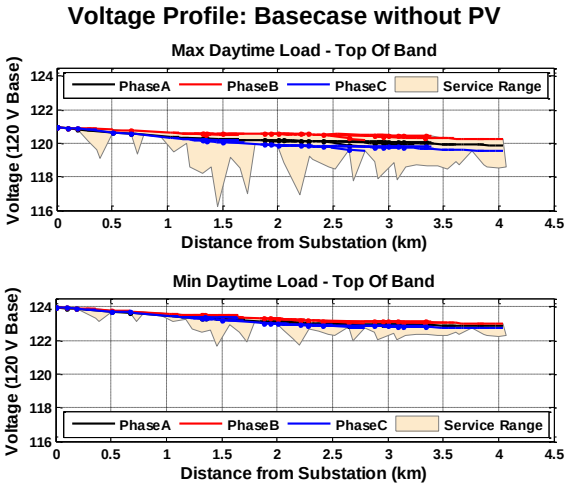




Ckt7

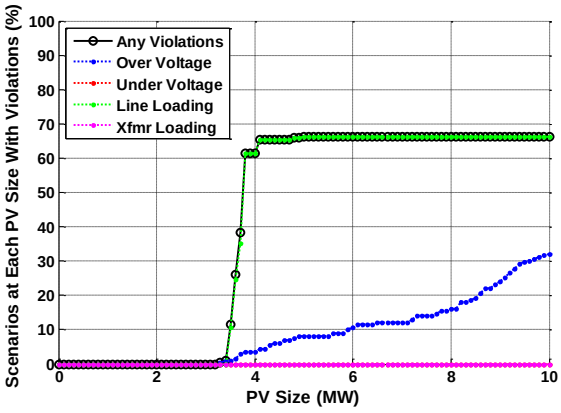


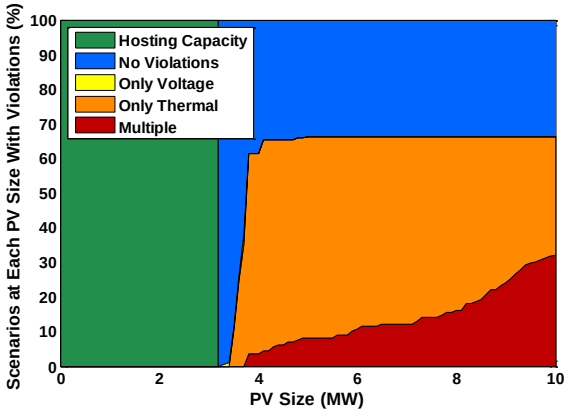
12.47 kV, 5.67 MW peak load
Max daytime load = 5.46 MW (96%)
Min daytime load = 2.27 MW (39%)



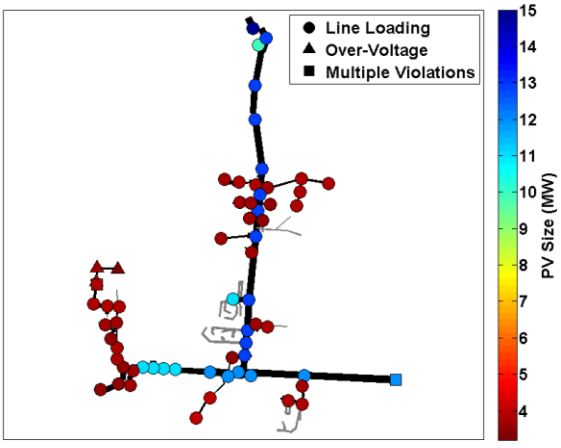
Bottom of Band bus voltages average 0.33V lower

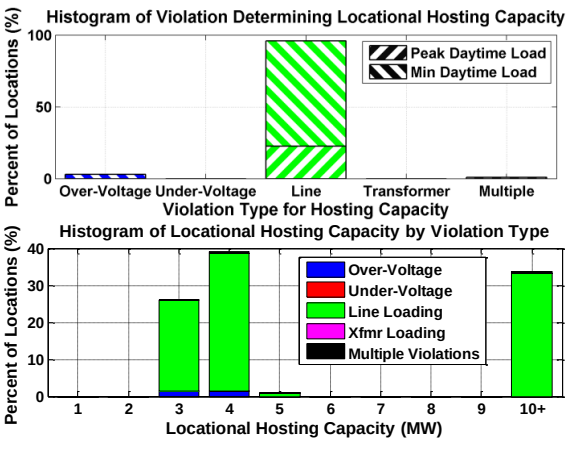
PV Impact Signature



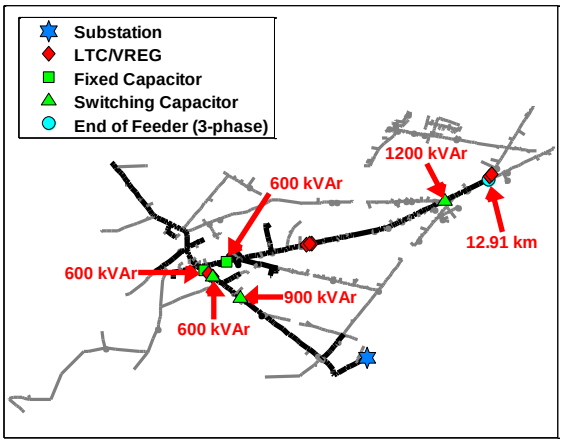


Locational Hosting Capacity

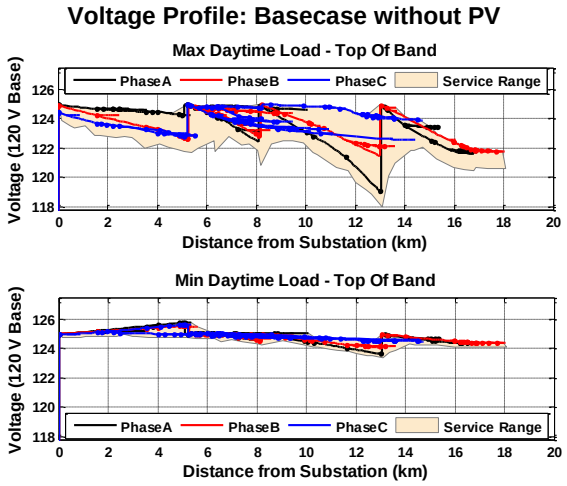




J1

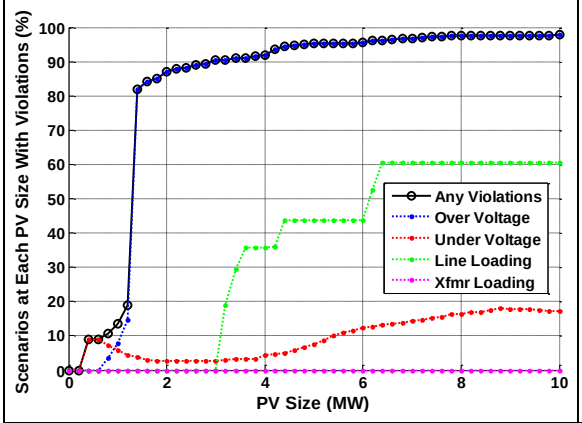


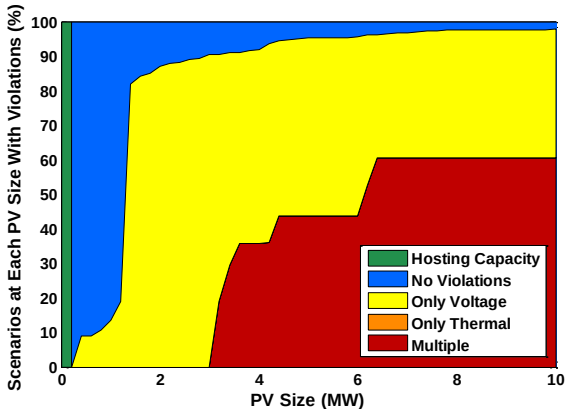
12.47 kV, 6.34 MW peak load
Max daytime load = 5.73 MW (90%)
Min daytime load = 1.04 MW (16%)



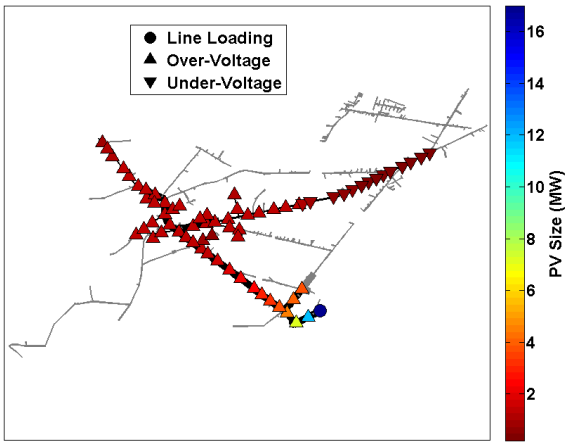
Bottom of Band bus voltages average 1.96V lower

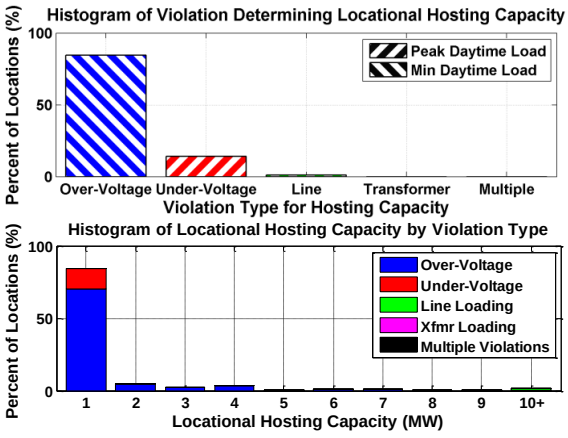
PV Impact Signature



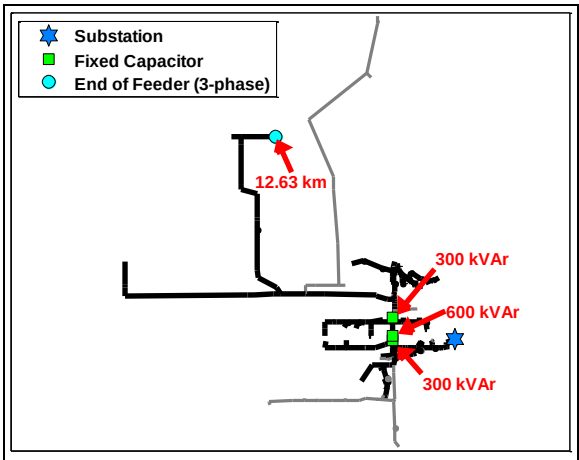


Locational Hosting Capacity

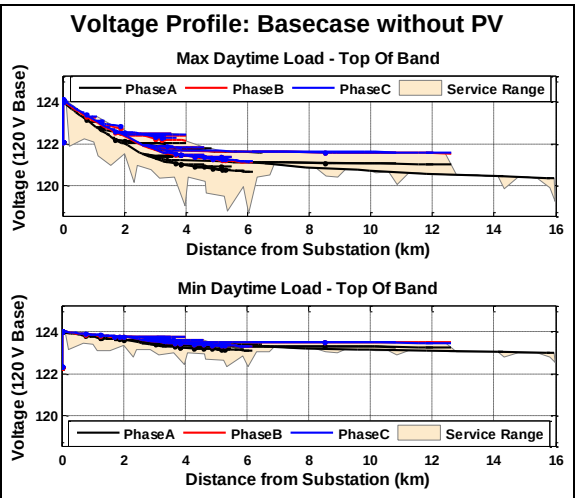




UT11

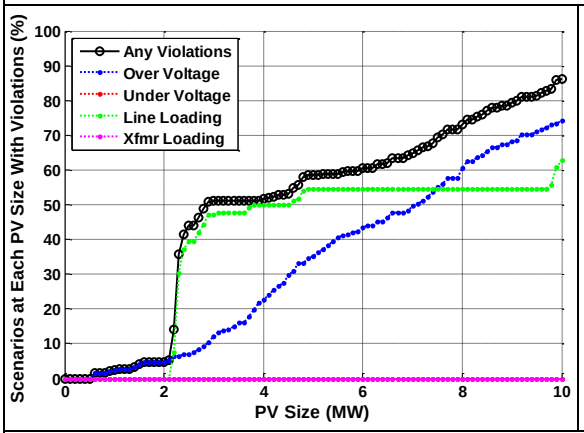


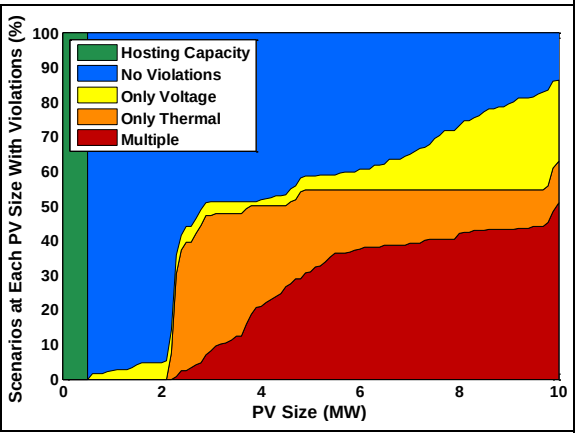
12.47 kV, 7.07 MW peak load
Max daytime load = 6.12 MW (86%)
Min daytime load = 2.58 MW (34%)



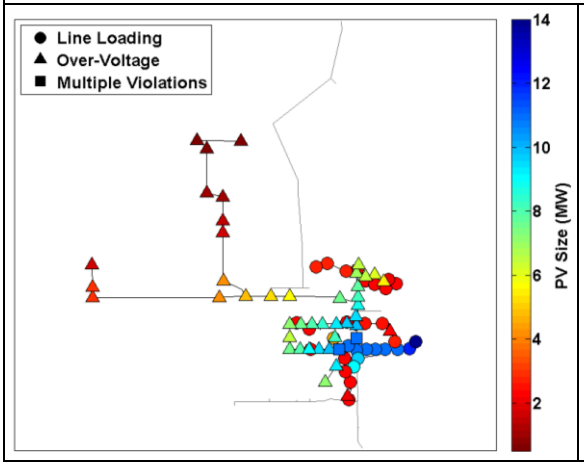
Bottom of Band bus voltages average 1.90V lower

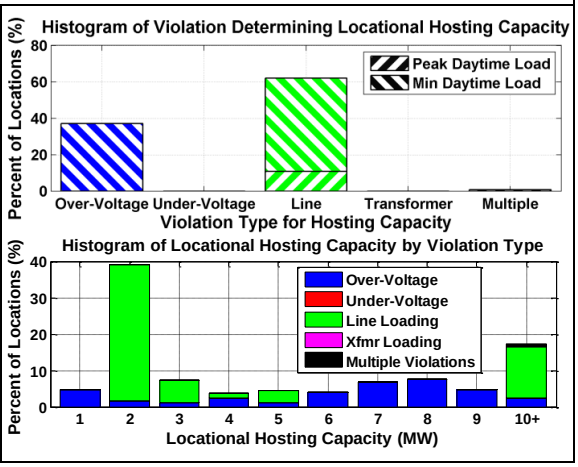
PV Impact Signature



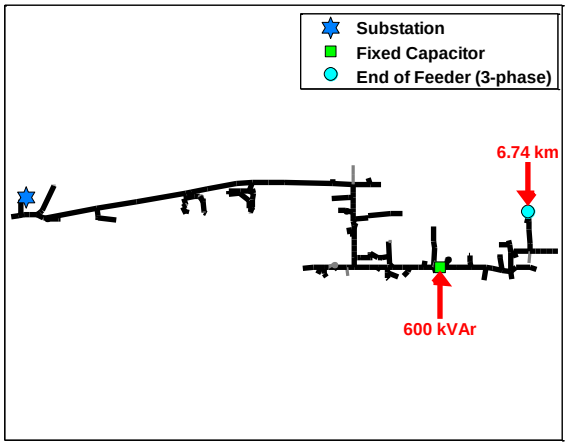


Locational Hosting Capacity

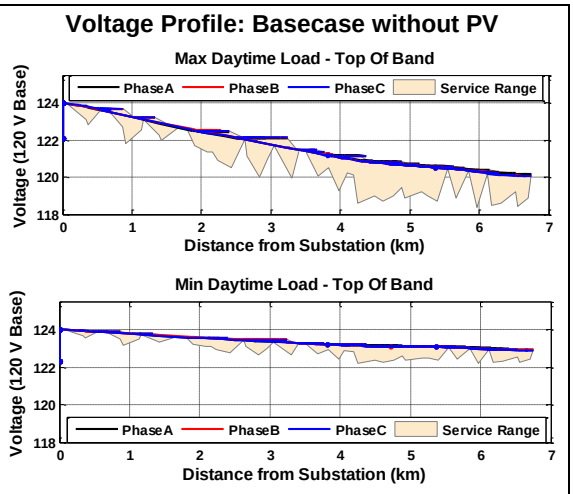




UT13

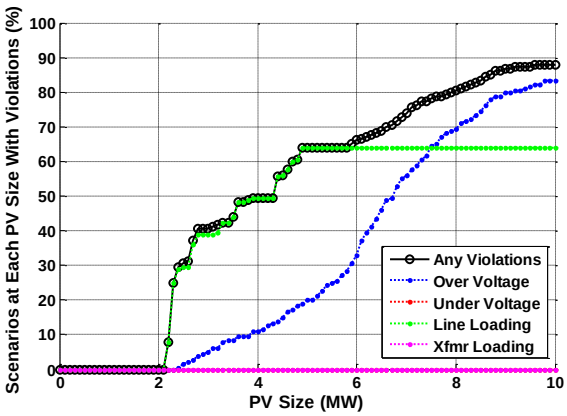


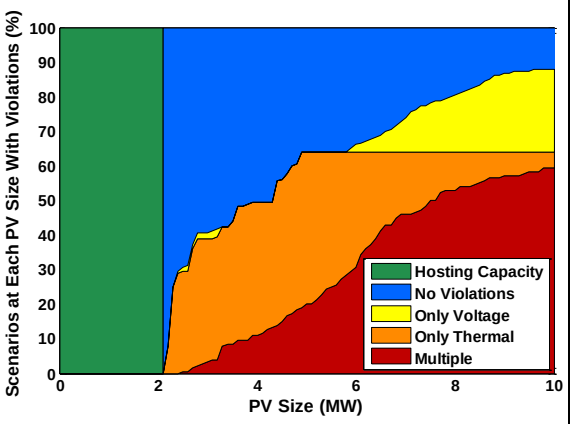
12.47 kV, 5.14 MW peak load
Max daytime load = 4.45 MW (86%)
Min daytime load = 1.85 MW (34%)



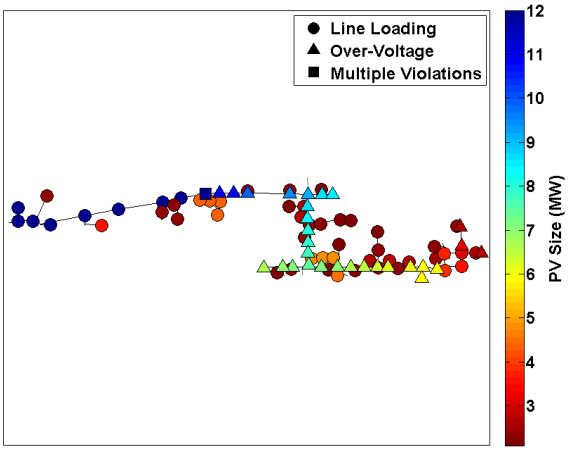
Bottom of Band bus voltages average 1.89V lower

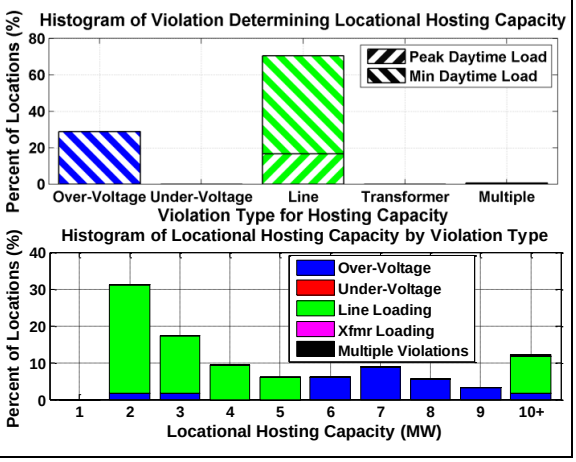
PV Impact Signature



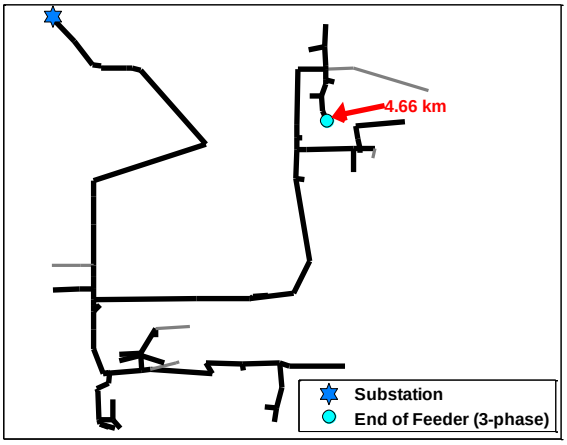


Locational Hosting Capacity

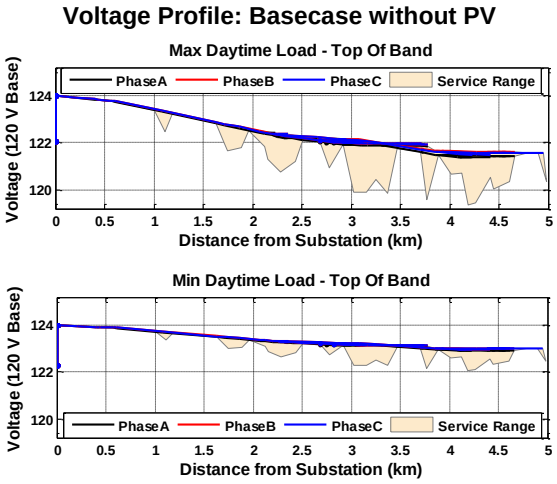




UT16

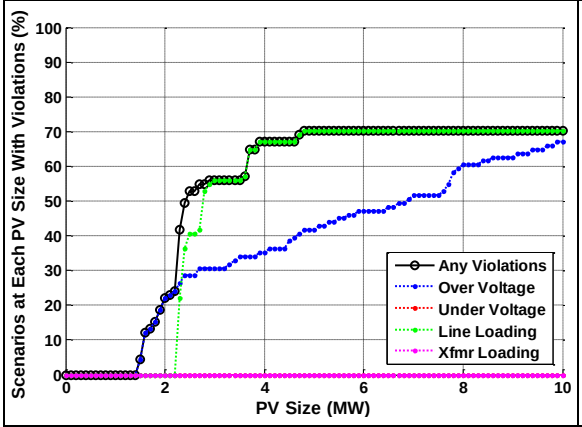


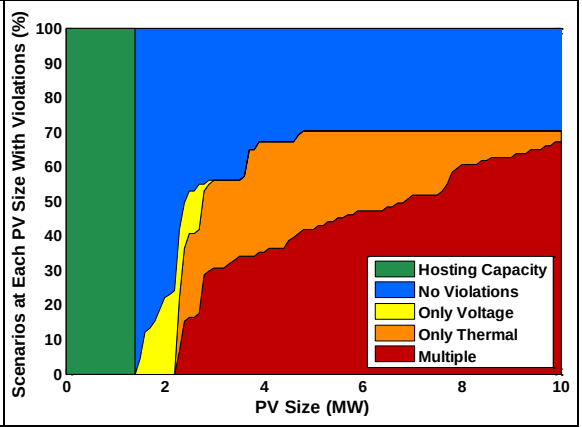
12.47 kV, 3.98 MW peak load
Max daytime load = 3.56 MW (89%)
Min daytime load = 1.51 MW (36%)



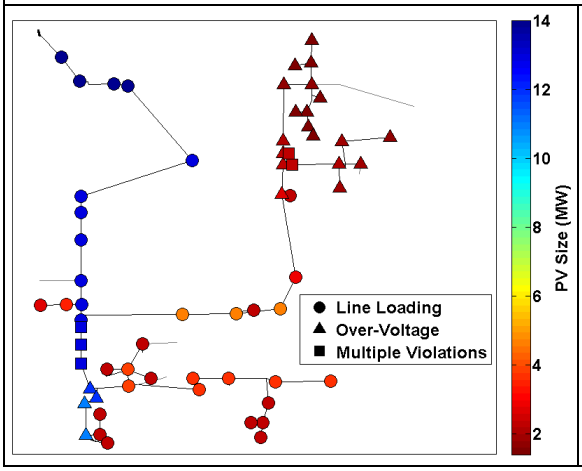
Bottom of Band bus voltages average 1.85V lower

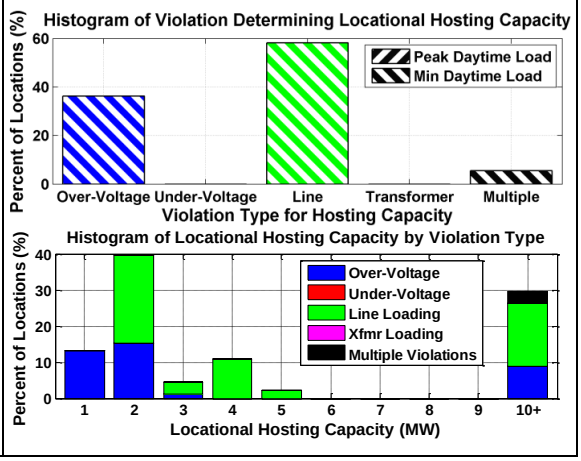
PV Impact Signature



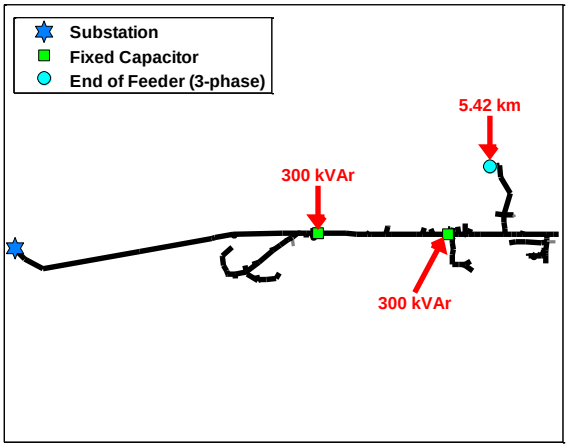


Locational Hosting Capacity



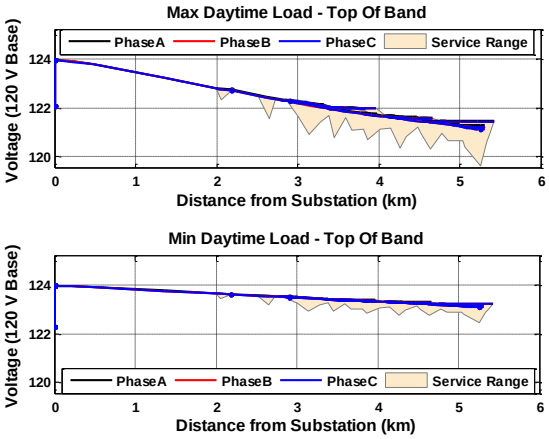


UT18



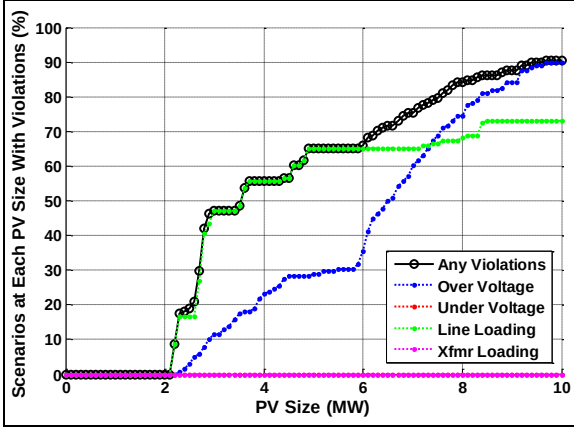
12.47 kV, 4.18 MW peak load
Max daytime load = 3.76 MW (89%)
Min daytime load = 1.65 MW (36%)

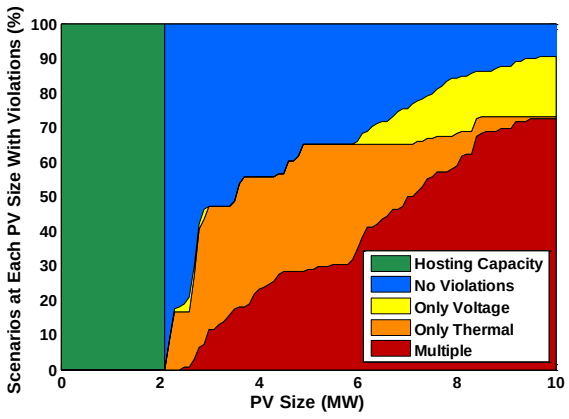
Voltage Profile: Basecase without PV



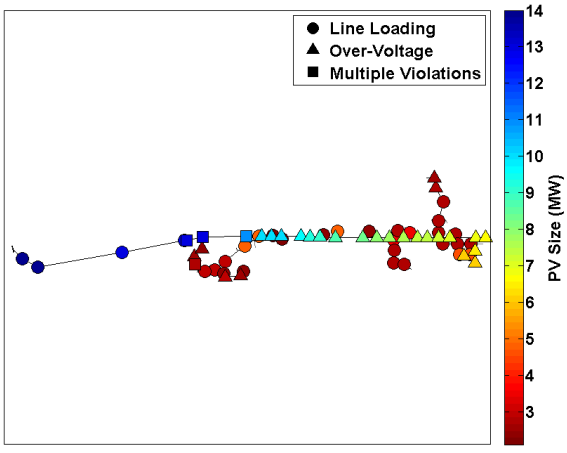
Bottom of Band bus voltages average 1.88V lower

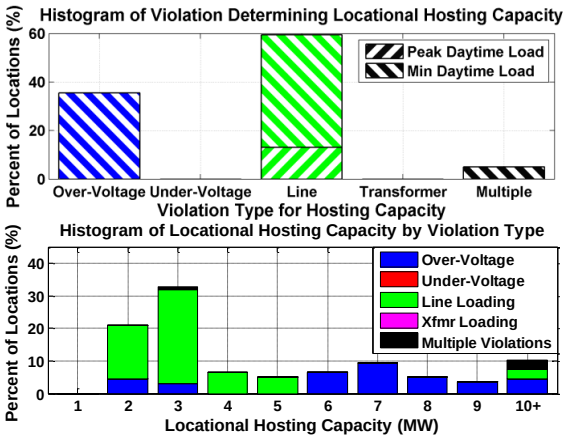
PV Impact Signature



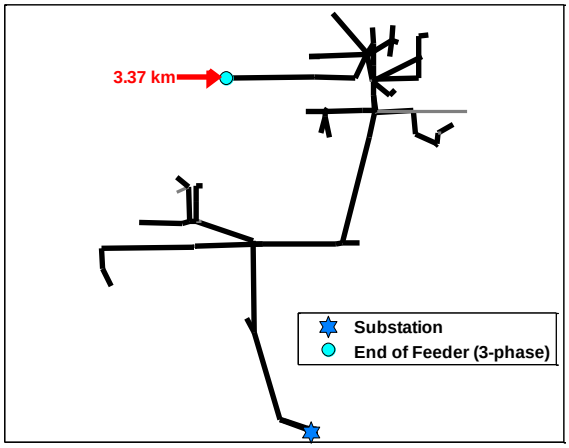


Locational Hosting Capacity

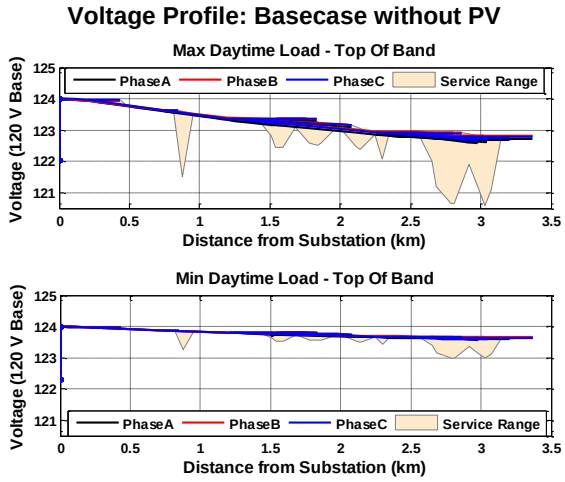




UT19

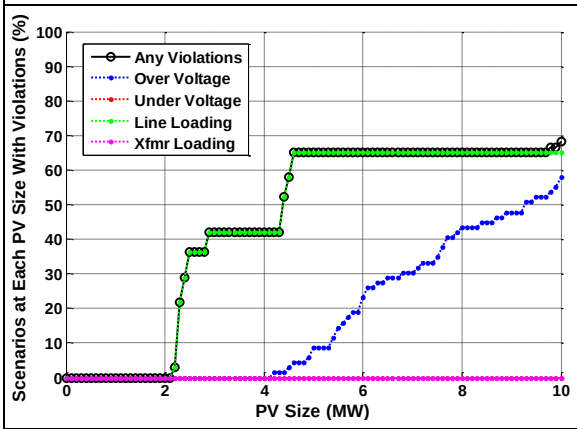


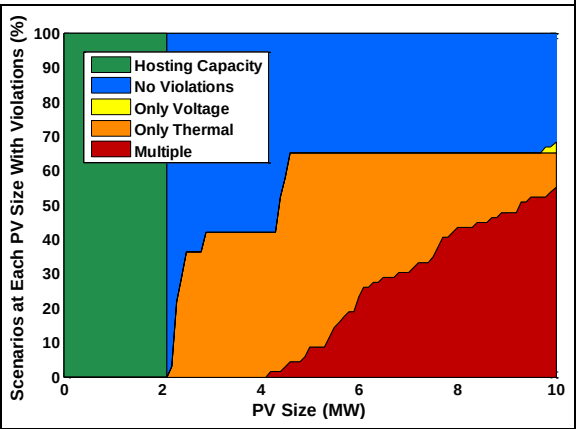
12.47 kV, 2.70 MW peak load
Max daytime load = 2.70 MW (100%)
Min daytime load = 0.86 MW (30%)



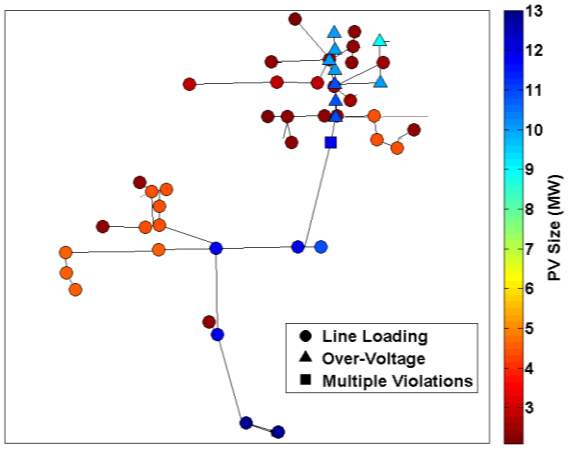
Bottom of Band bus voltages average 1.84V lower

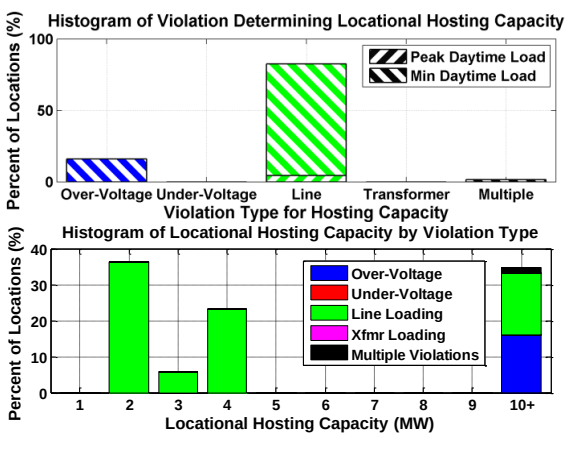
PV Impact Signature



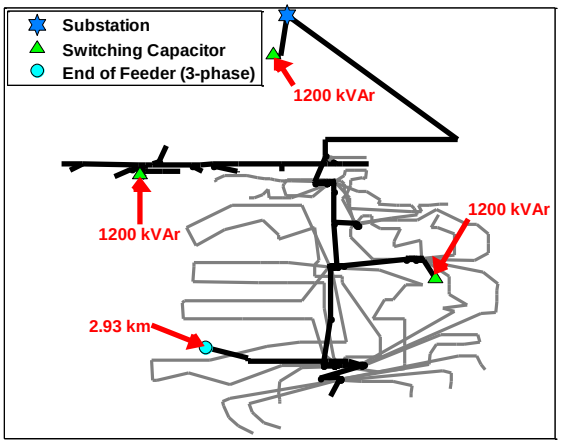


Locational Hosting Capacity

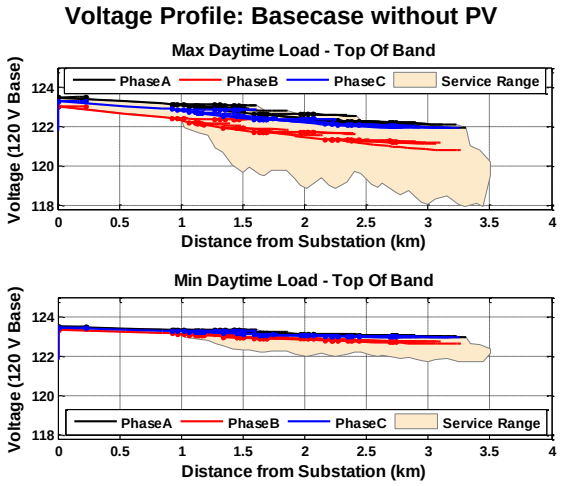




M1

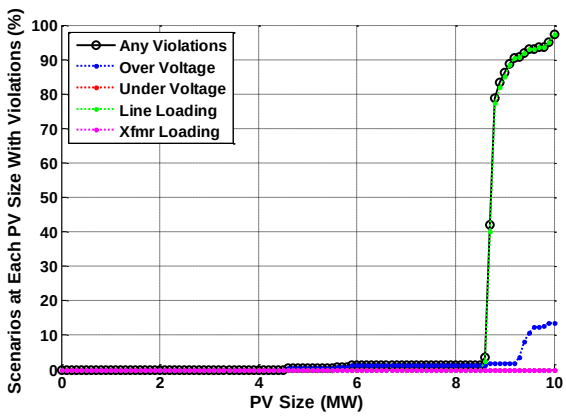


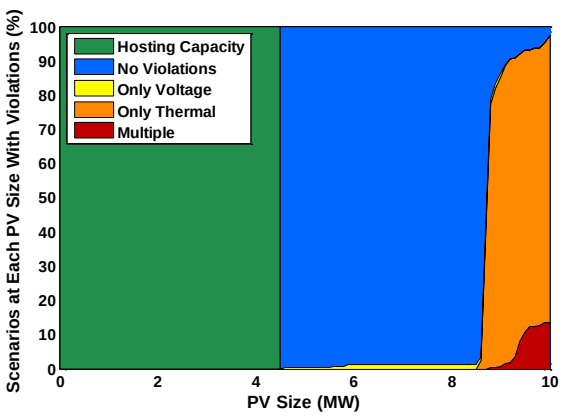
12.47 kV, 5.82 MW peak load
Max daytime load = 5.53 MW (95%)
Min daytime load = 1.65 MW (28%)



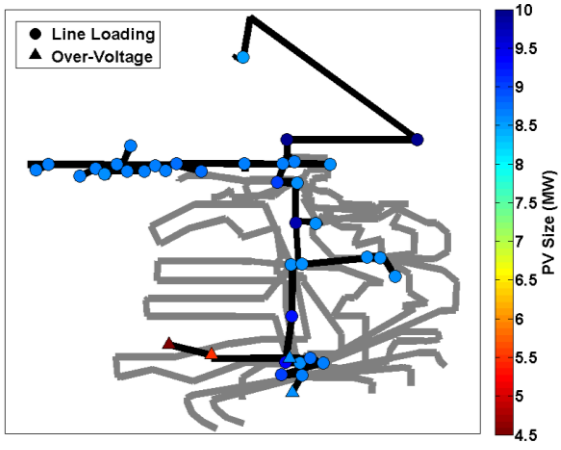
Bottom of Band bus voltages average 2.96V lower

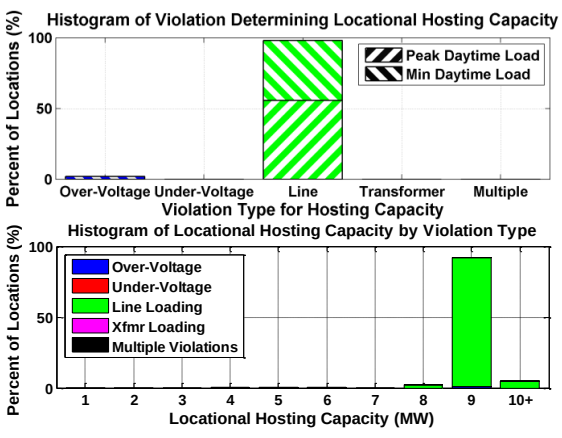
PV Impact Signature



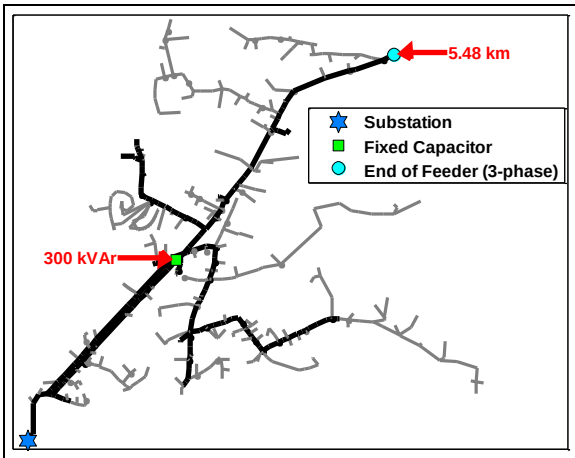


Locational Hosting Capacity

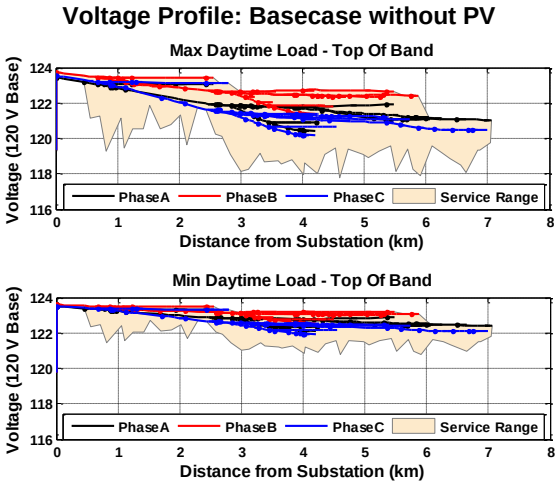




K1

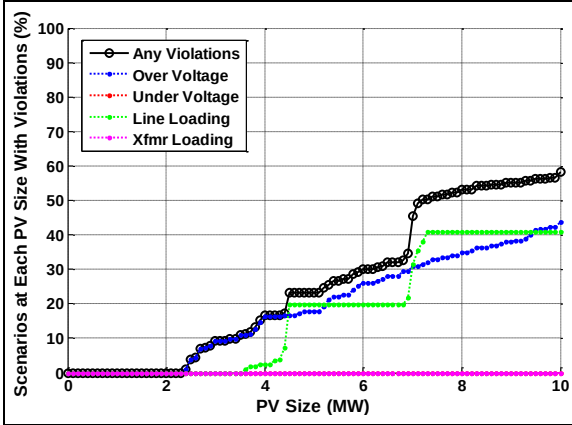


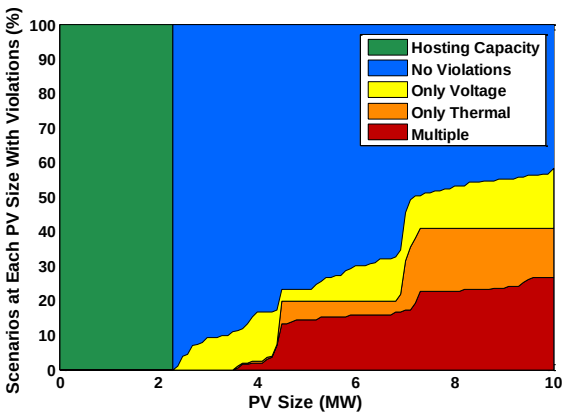
13.2 kV, 4.86 MW peak load
Max daytime load = 4.63 MW (95%)
Min daytime load = 1.38 MW (28%)



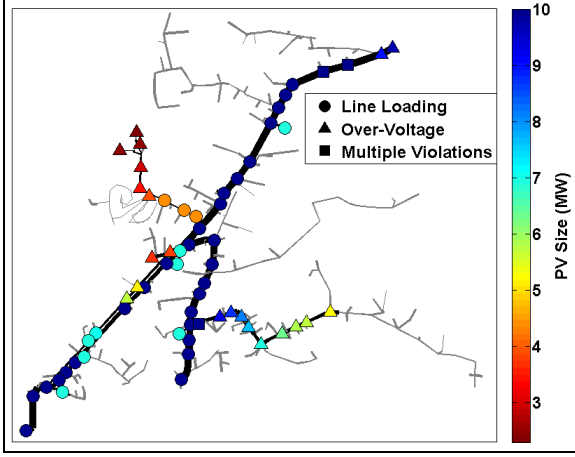
Bottom of Band bus voltages average 2.07V lower

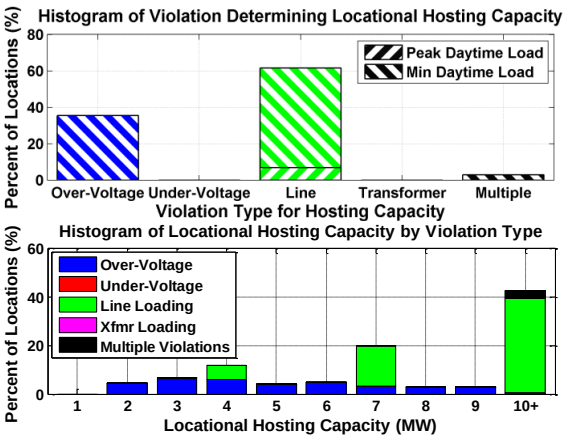
PV Impact Signature



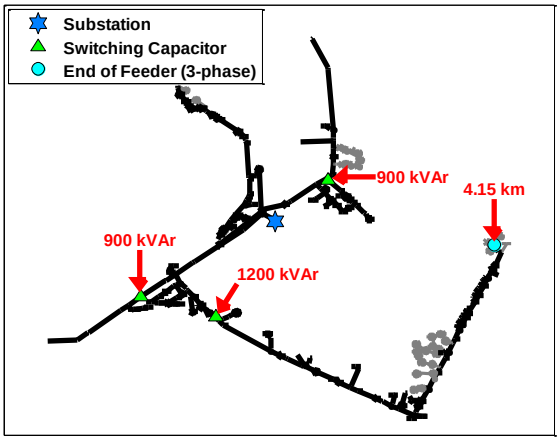


Locational Hosting Capacity



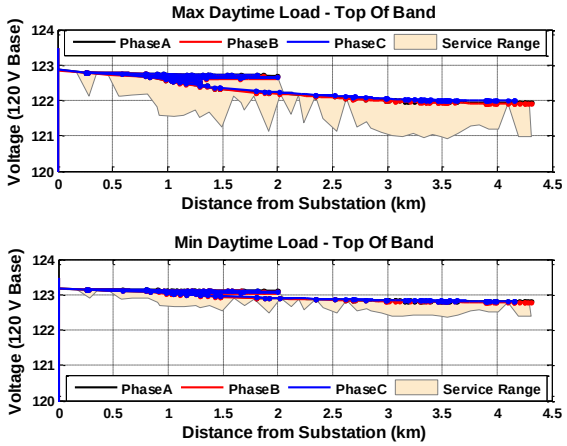


CL1



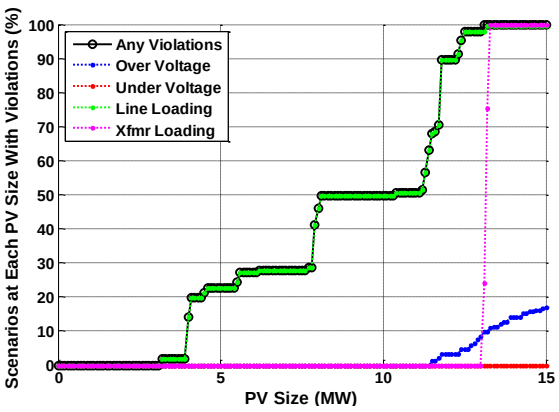
16 kV, 5.87 MW peak load
Max daytime load = 5.21 MW (89%)
Min daytime load = 1.97 MW (33%)

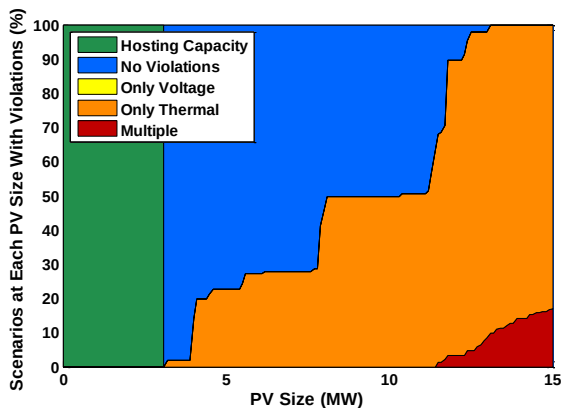
Voltage Profile: Basecase without PV



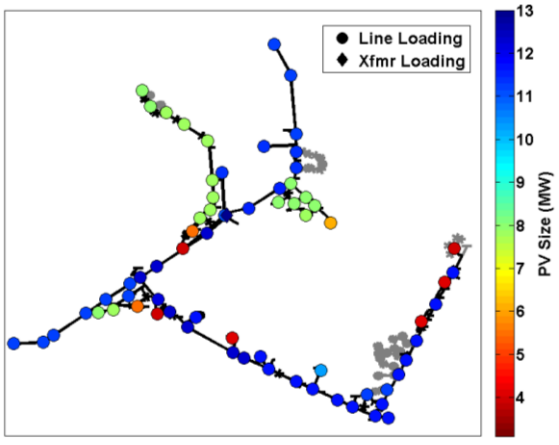
Bottom of Band bus voltages average 2.09 V lower

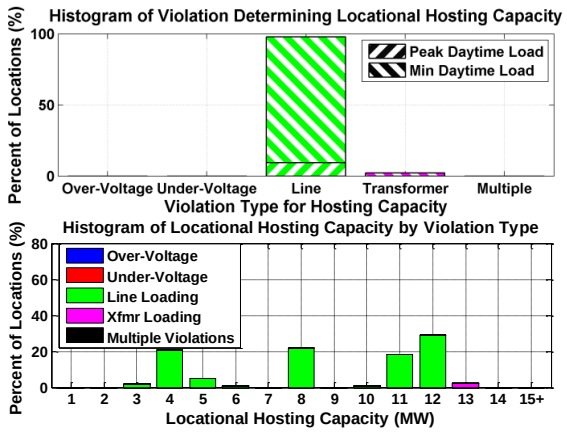
PV Impact Signature



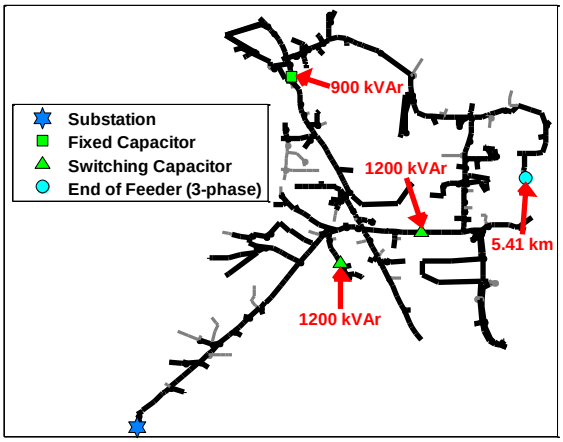


Locational Hosting Capacity

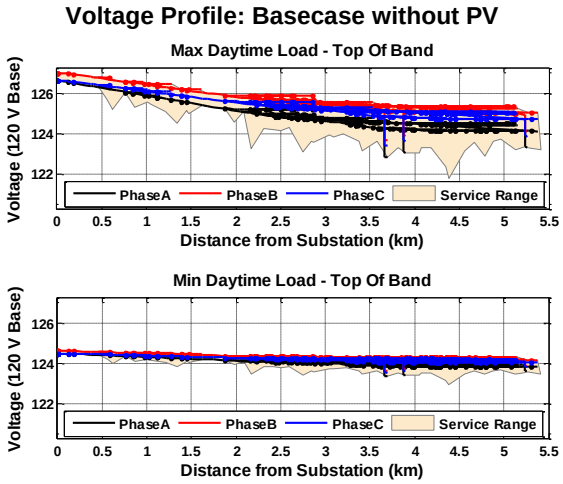




ML1

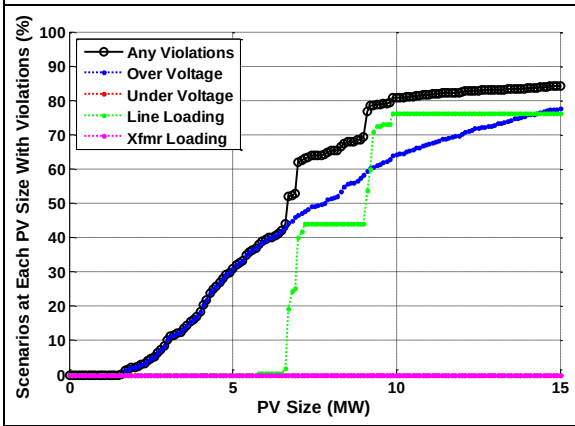


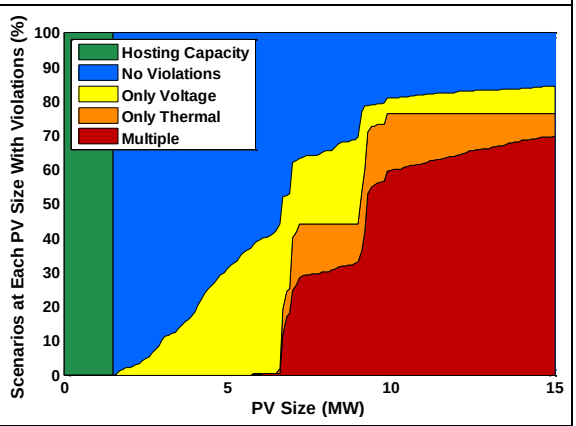
19.8 kV, 6.93 MW peak load
Max daytime load = 6.93 MW (100%)
Min daytime load = 2.52 MW (36%)



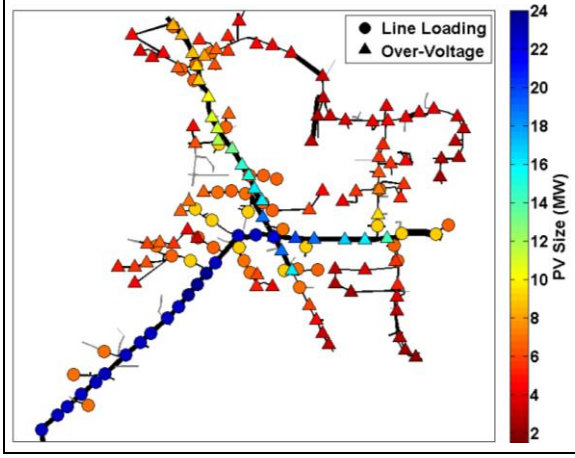
Bottom of Band bus voltages average 2.92V lower

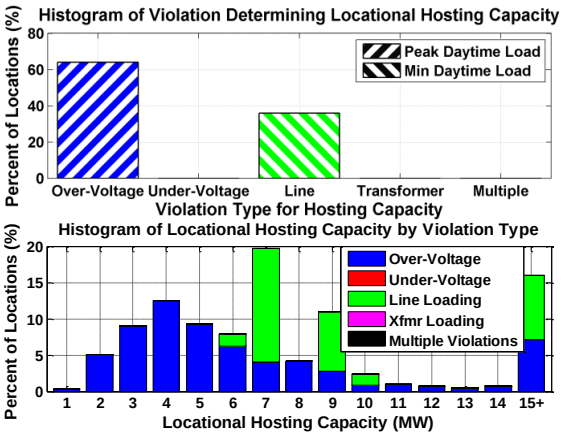
PV Impact Signature



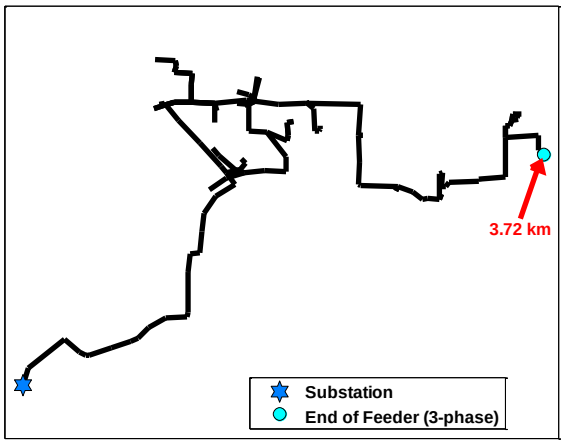


Locational Hosting Capacity

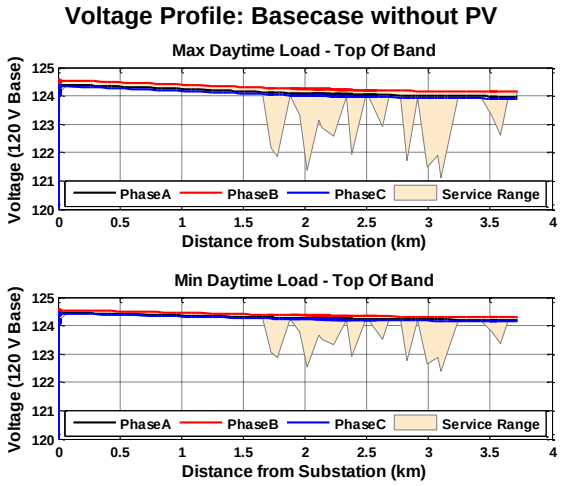




GL1

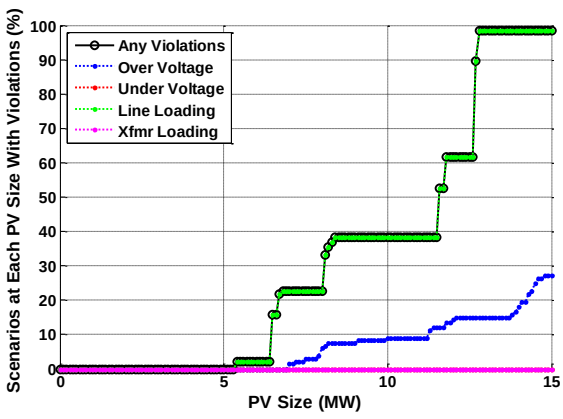


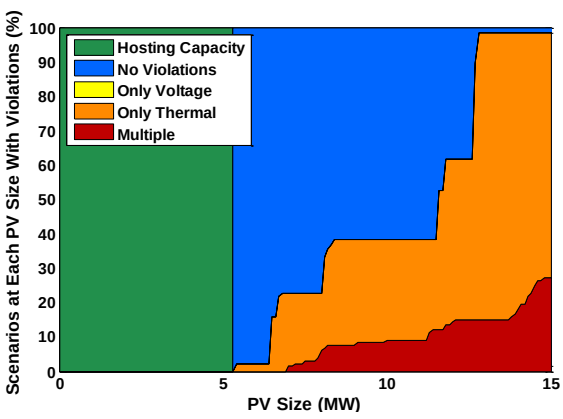
19.8 kV, 3.27 MW peak load
Max daytime load = 3.19 MW (97%)
Min daytime load = 2.05 MW (61%)



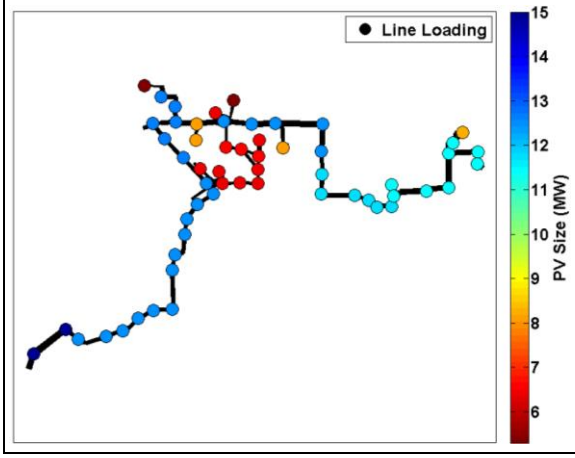
Bottom of Band bus voltages average 3.24V lower

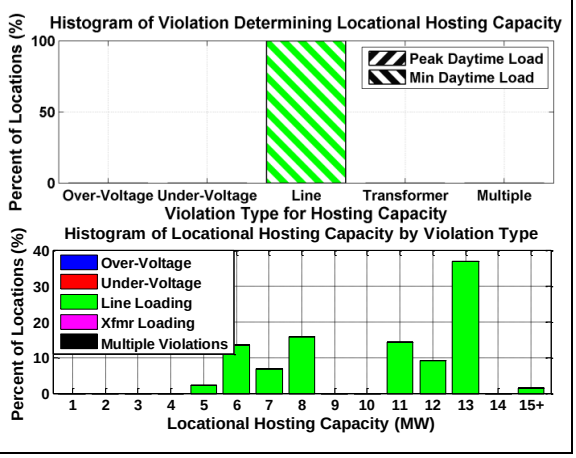
PV Impact Signature



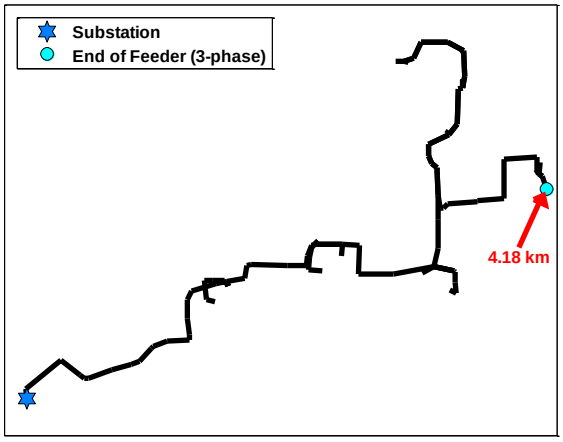


Locational Hosting Capacity

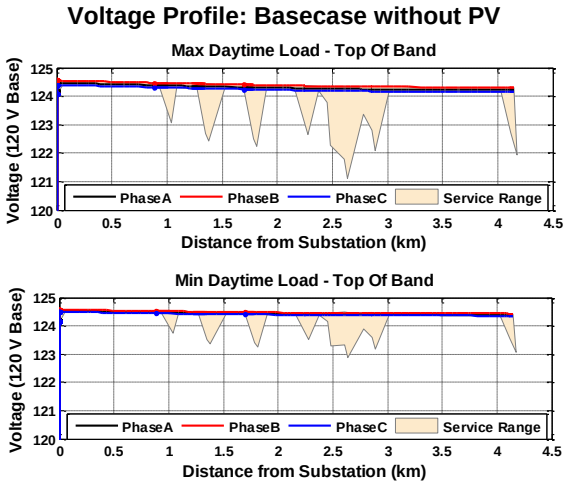




GL2

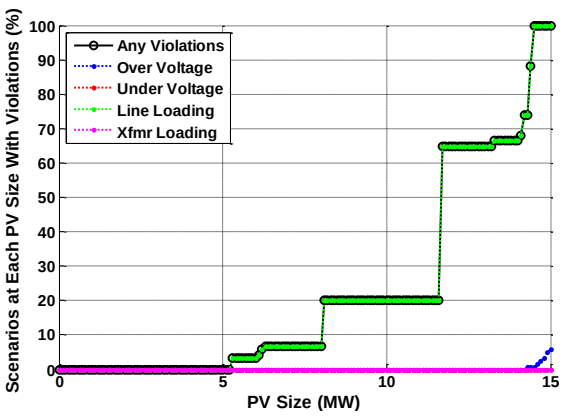


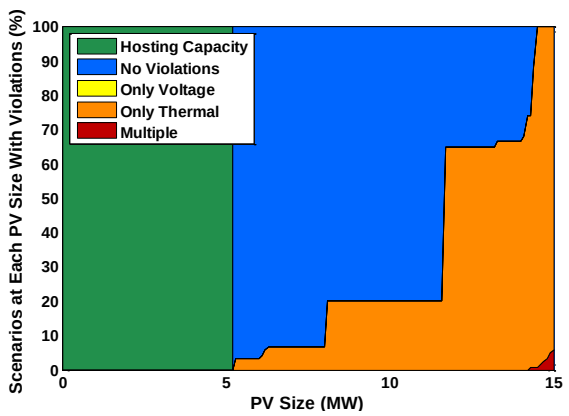
19.8 kV, 2.23 MW peak load
Max daytime load = 2.21 MW (99%)
Min daytime load = 1.28 MW (56%)



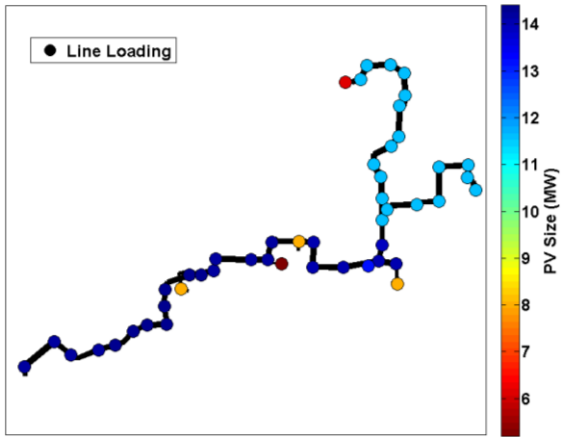
Bottom of Band bus voltages average 3.24V lower

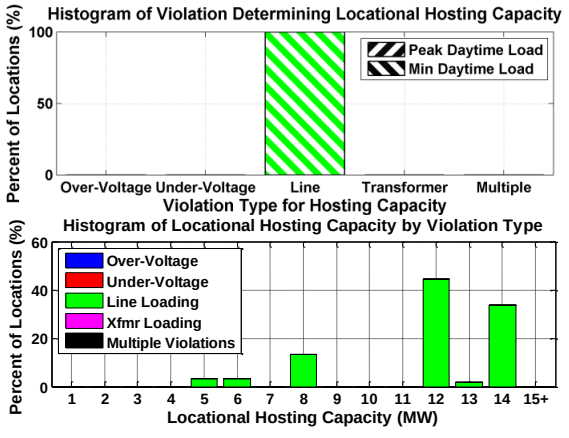
PV Impact Signature



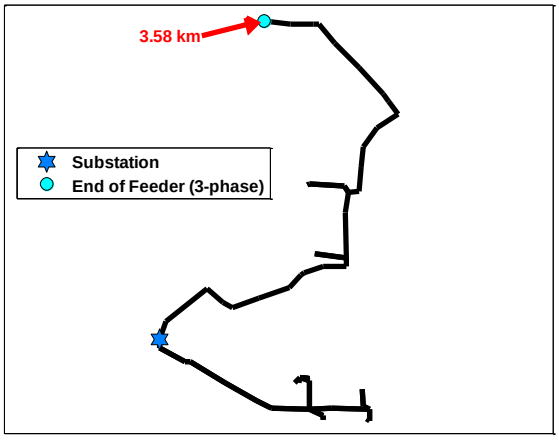


Locational Hosting Capacity

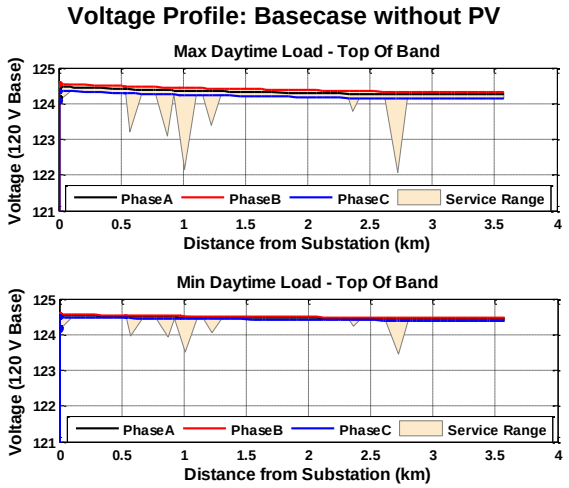




GL3

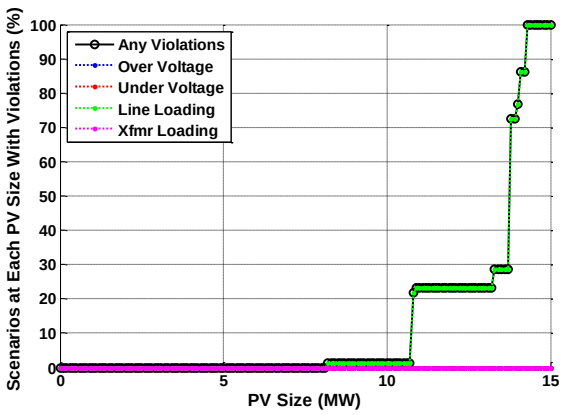


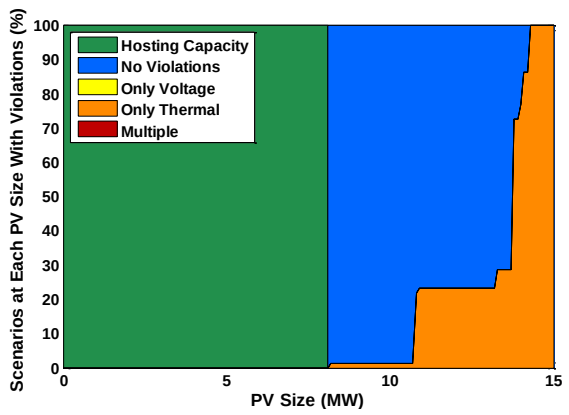
19.8 kV, 2.61 MW peak load
Max daytime load = 2.39 MW (91%)
Min daytime load = 1.08 MW (40%)



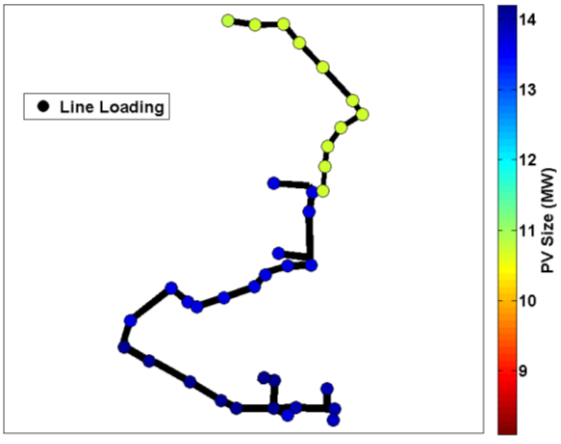
Bottom of Band bus voltages average 3.17V lower

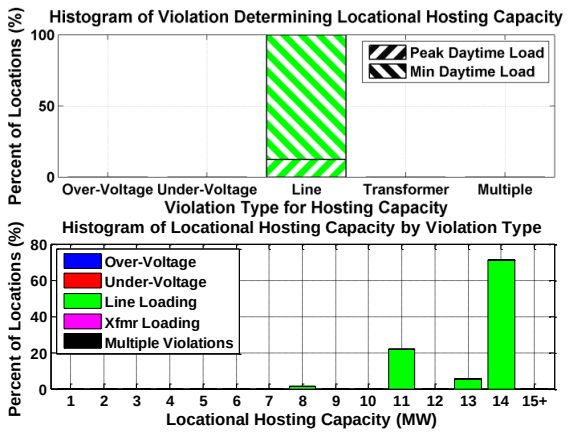
PV Impact Signature



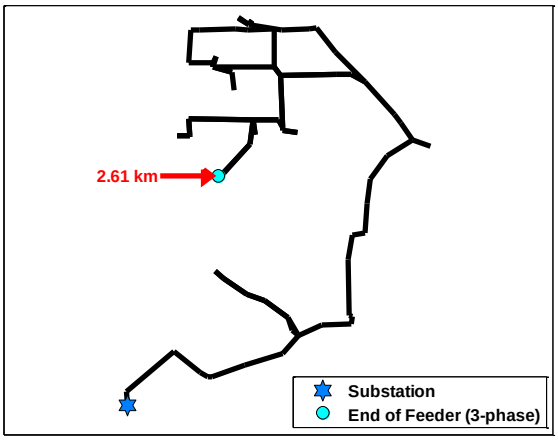


Locational Hosting Capacity

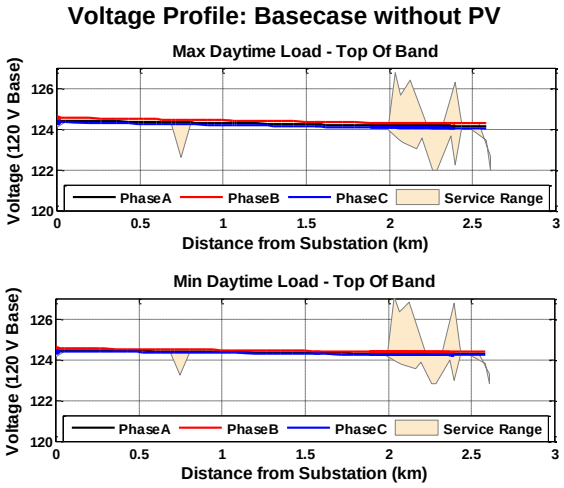




GL4

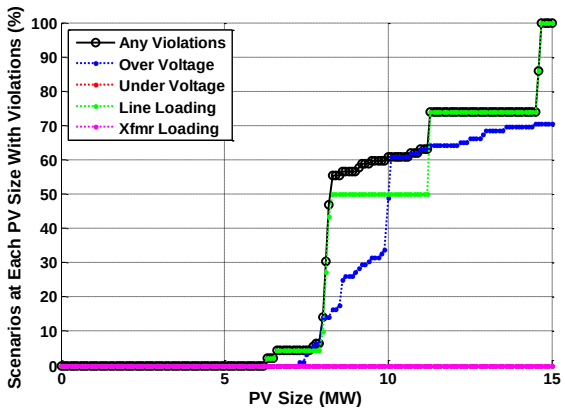


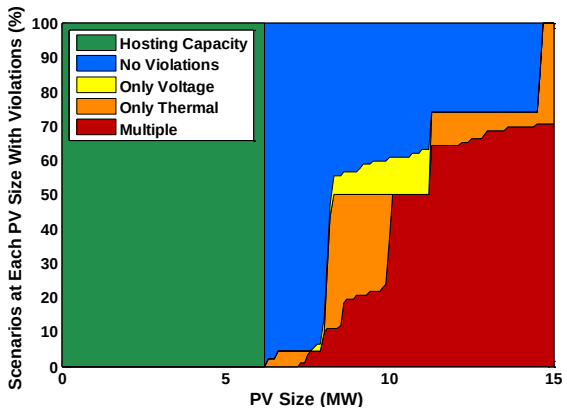
19.8 kV, 2.51 MW peak load
Max daytime load = 2.38 MW (95%)
Min daytime load = 1.62 MW (63%)



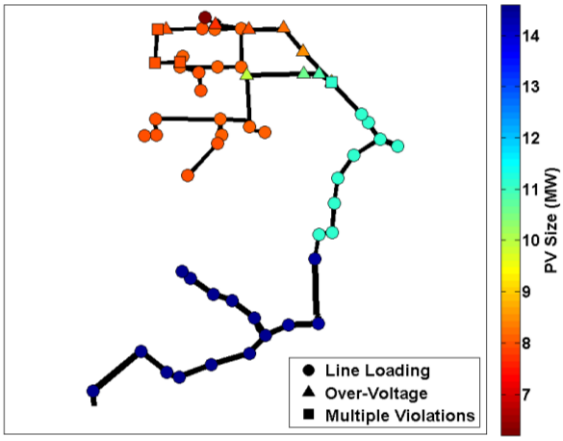
Bottom of Band bus voltages average 3.19V lower

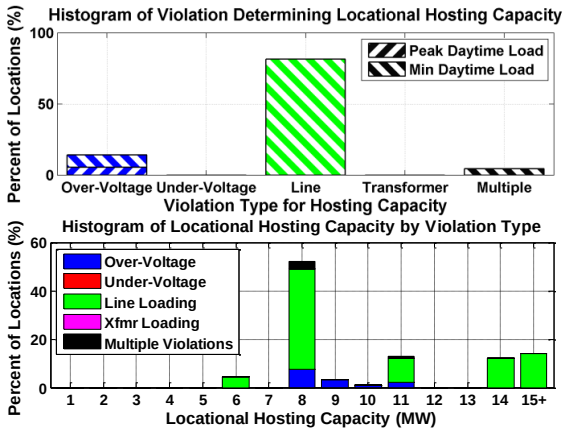
PV Impact Signature



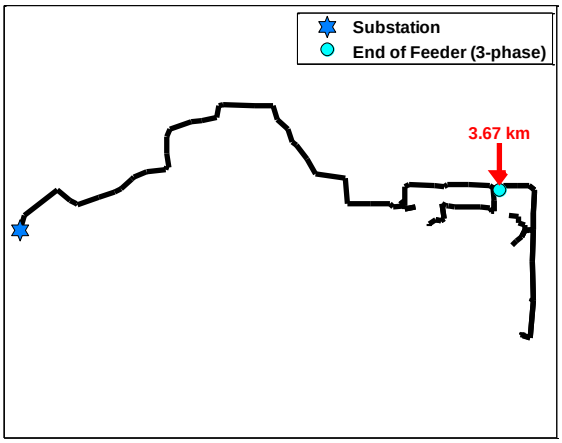


Locational Hosting Capacity

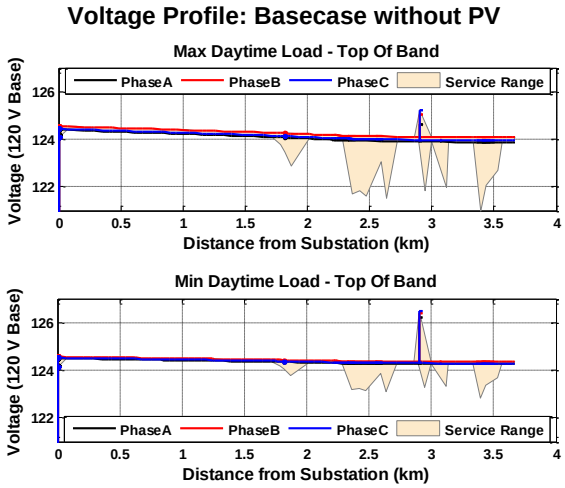




GL5

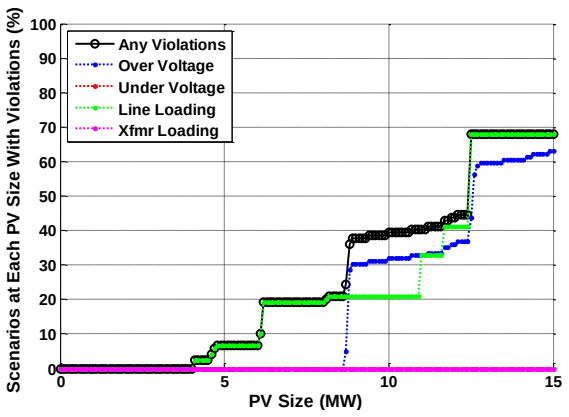


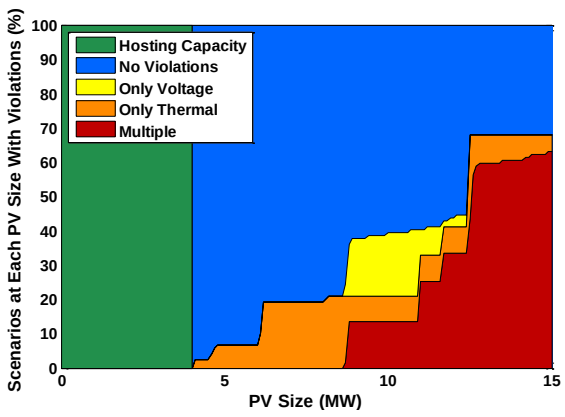
19.8 kV, 3.97 MW peak load
Max daytime load = 3.86 MW (97%)
Min daytime load = 1.91 MW (47%)



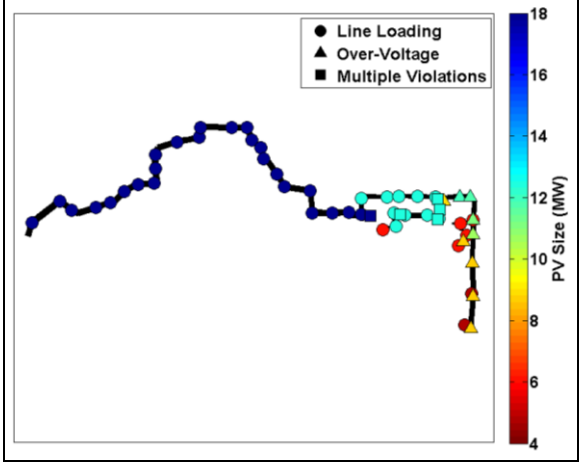
Bottom of Band bus voltages average 3.24V lower

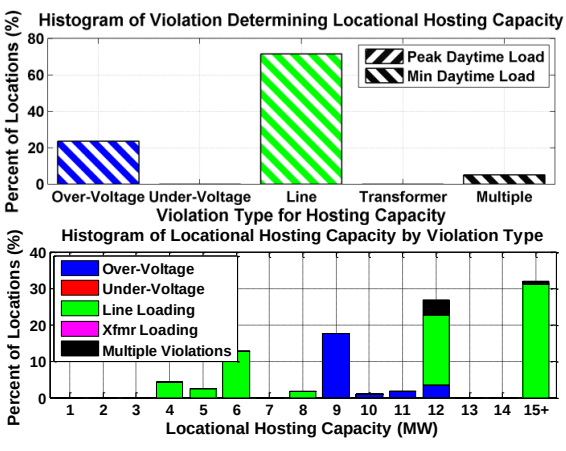
PV Impact Signature



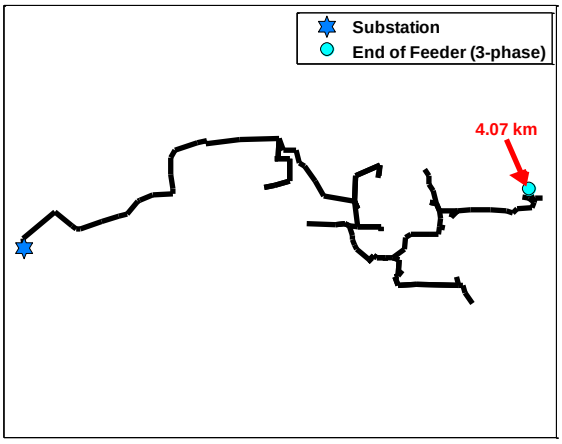


Locational Hosting Capacity

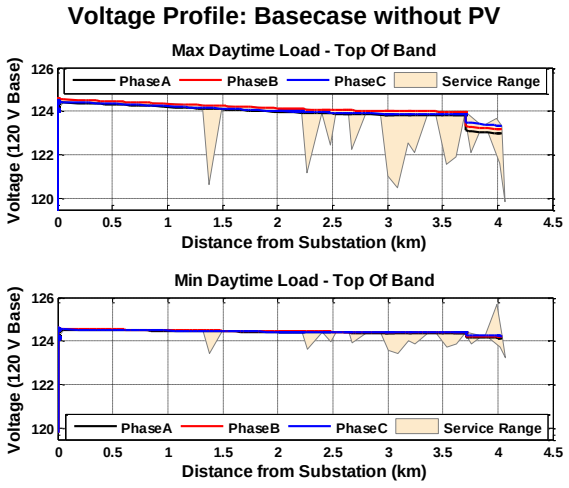




GL6

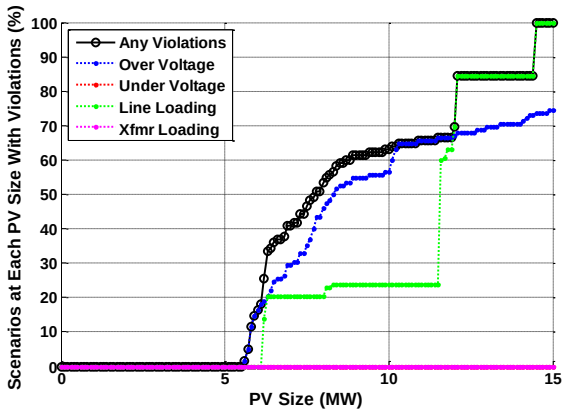


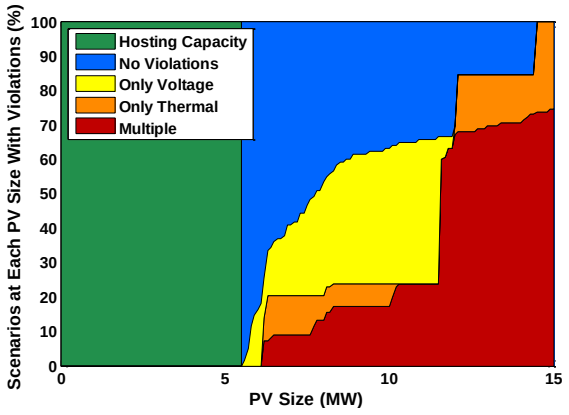
19.8 / 4.16 kV (19.8 kV analyzed), 4.75 MW peak load
Max daytime load = 4.67 MW (98%)
Min daytime load = 1.35 MW (28%)



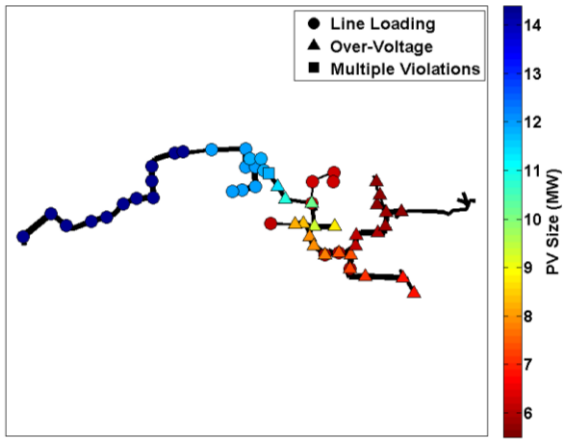
Bottom of Band bus voltages average 3.25V lower

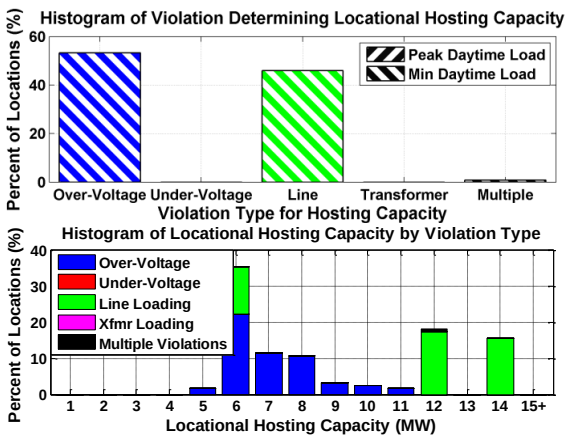
PV Impact Signature



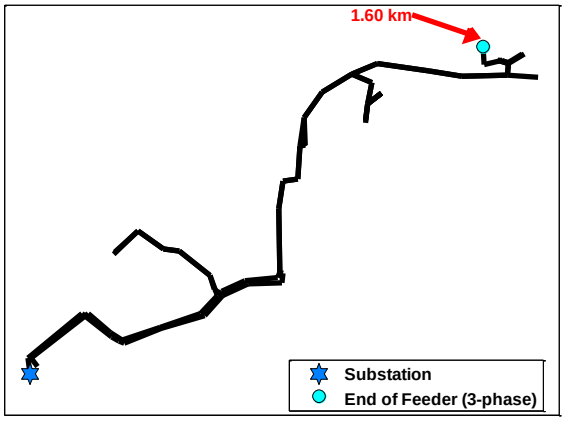


Locational Hosting Capacity

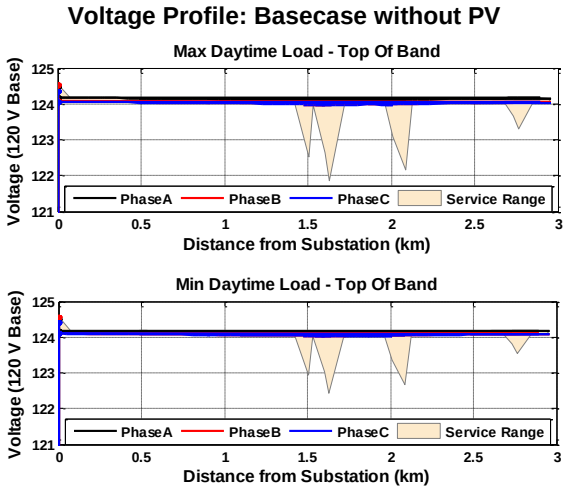




GN1

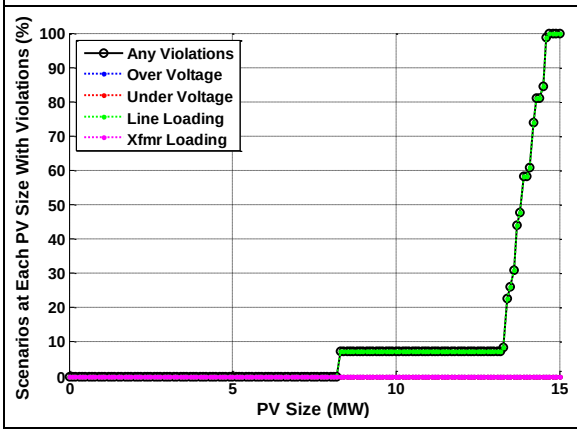


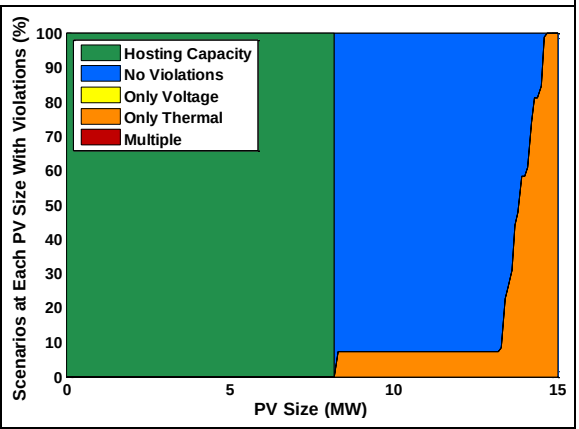
19.8 kV, 2.86 MW peak load
Max daytime load = 2.85 MW (99%)
Min daytime load = 2.16 MW (75%)



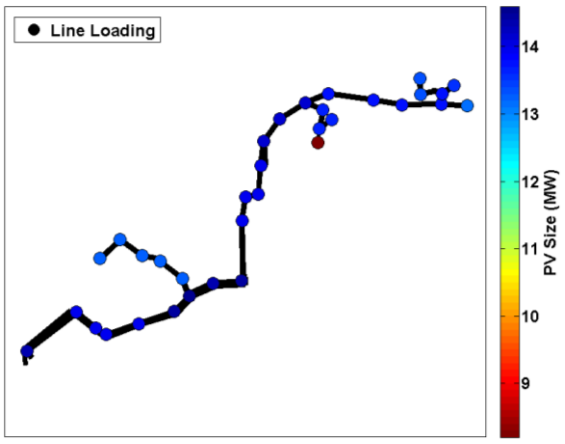
Bottom of Band bus voltages average 2.48 V lower

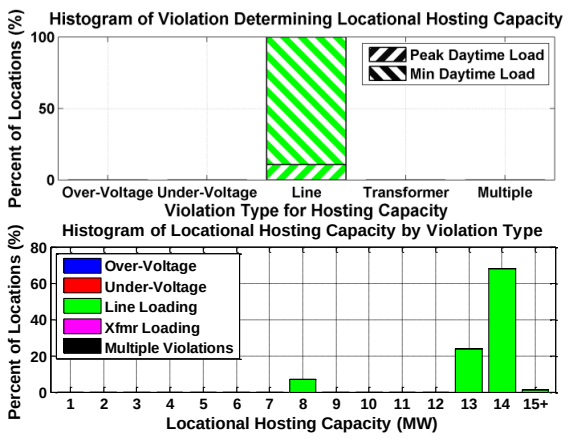
PV Impact Signature



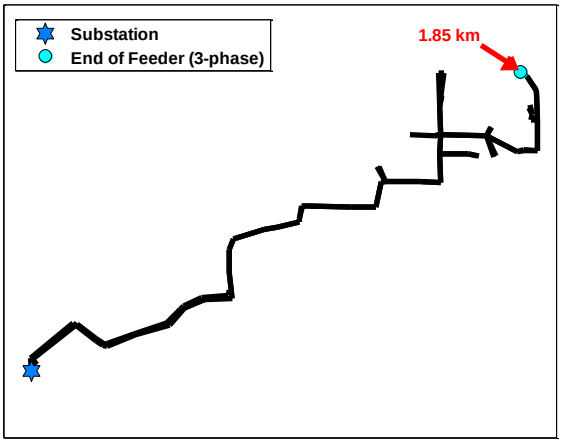


Locational Hosting Capacity

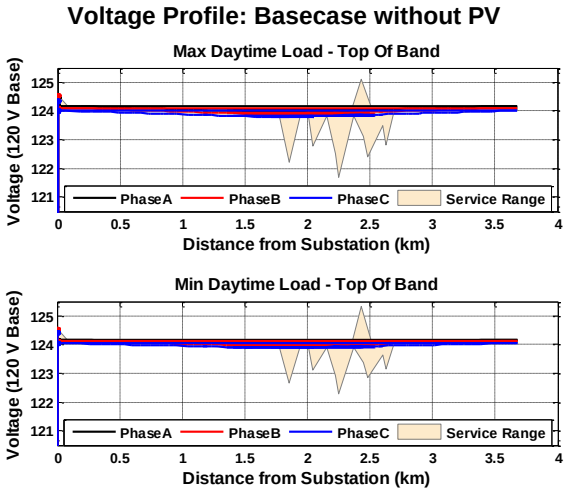




GN3

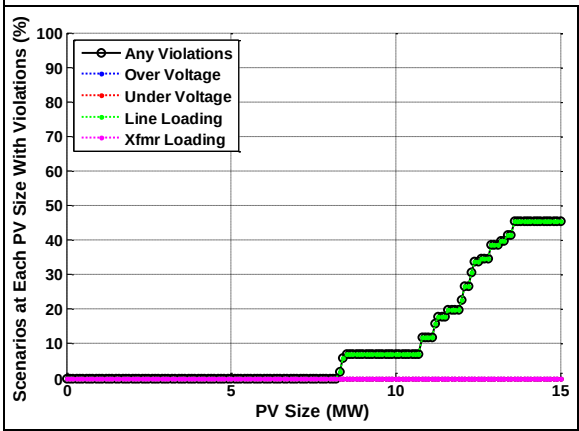


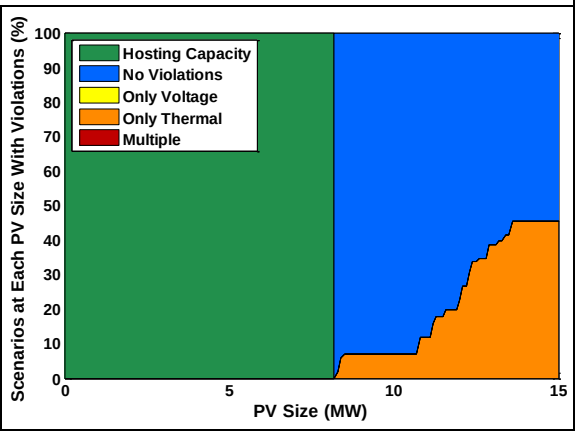
19.8 kV, 5.55 MW peak load
Max daytime load = 5.53 MW (99%)
Min daytime load = 4.23 MW (75%)



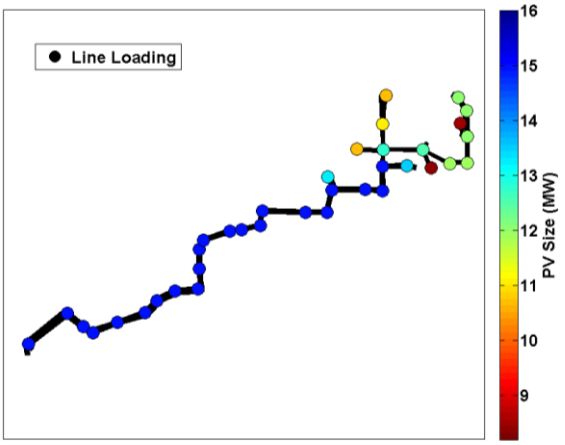
Bottom of Band bus voltages average 2.47 V lower

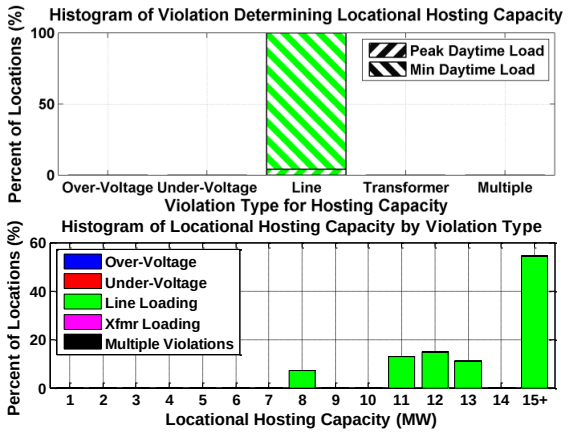
PV Impact Signature



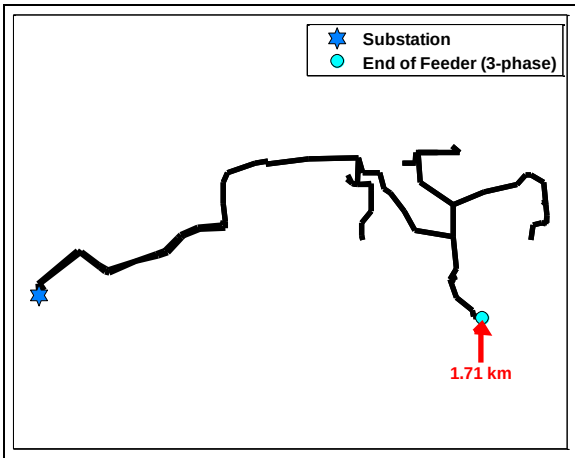


Locational Hosting Capacity

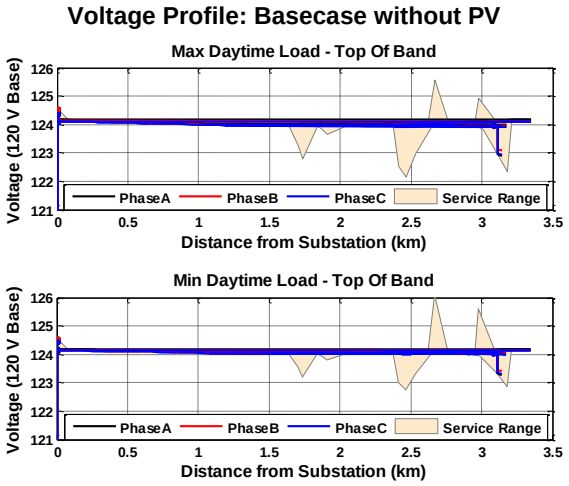




GN5

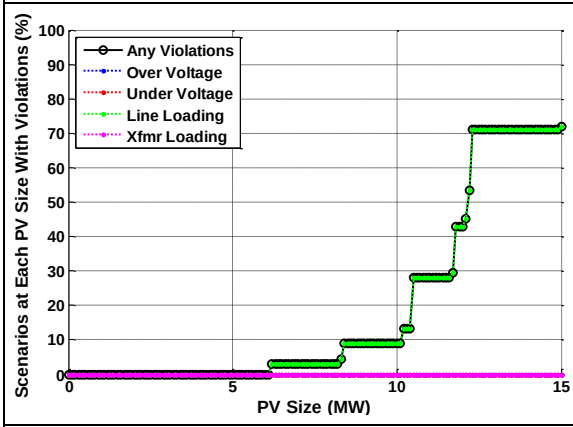


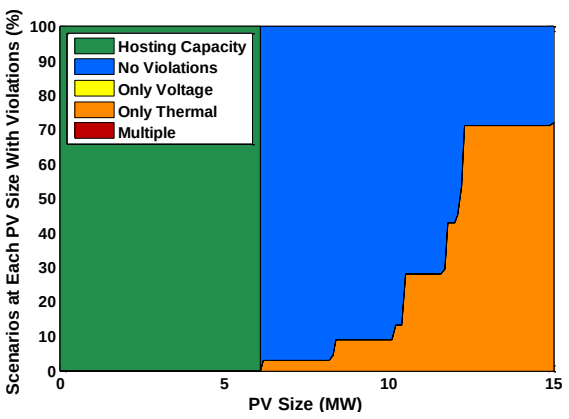
19.8 kV, 5.06 MW peak load
Max daytime load = 5.05 MW (100%)
Min daytime load = 3.61 MW (70%)



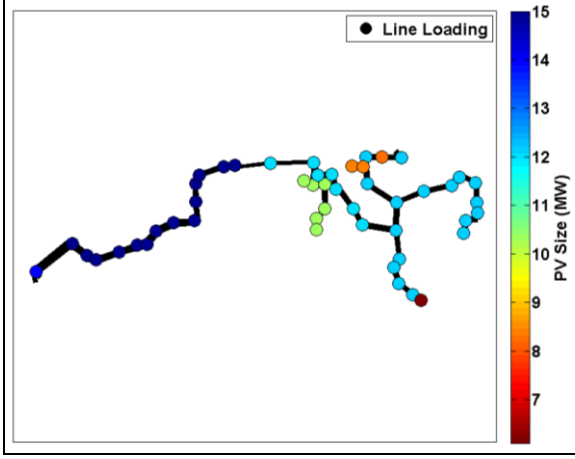
Bottom of Band bus voltages average 2.46 V lower

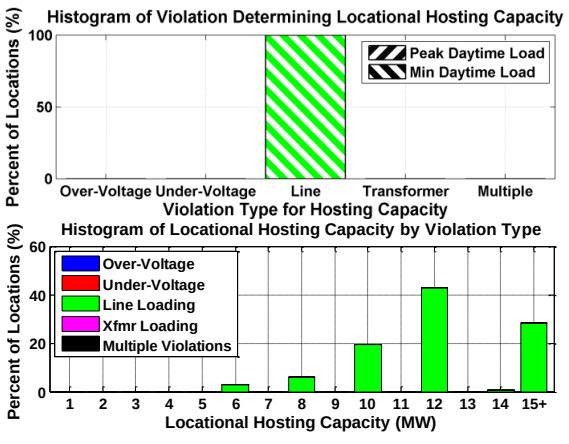
PV Impact Signature



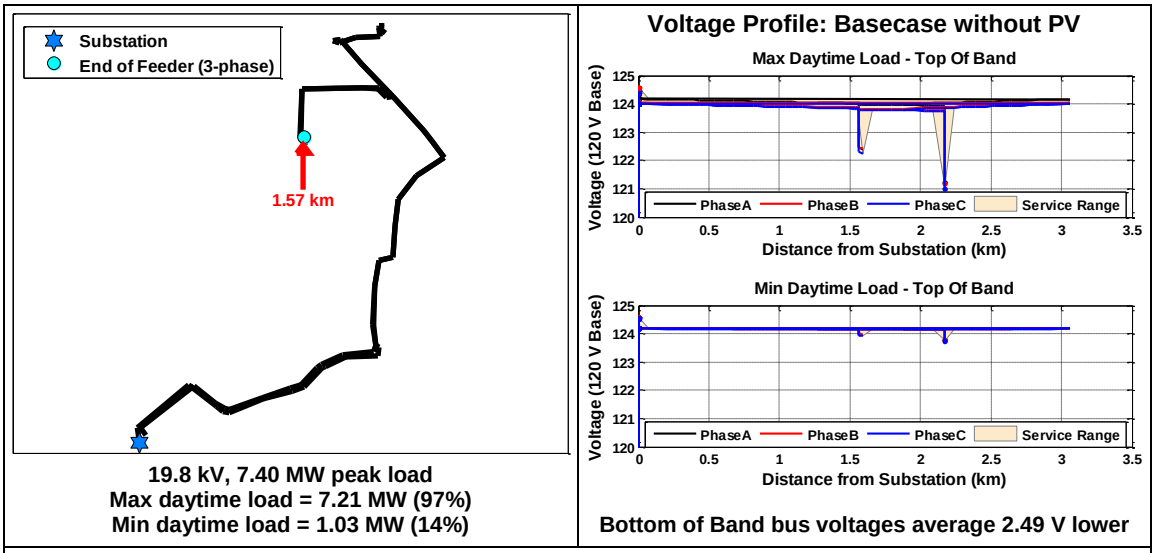


Locational Hosting Capacity

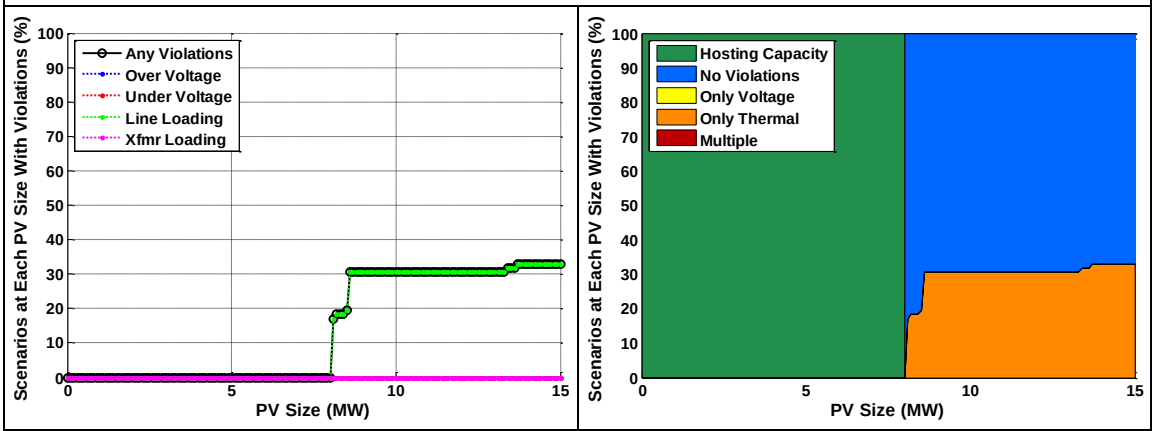




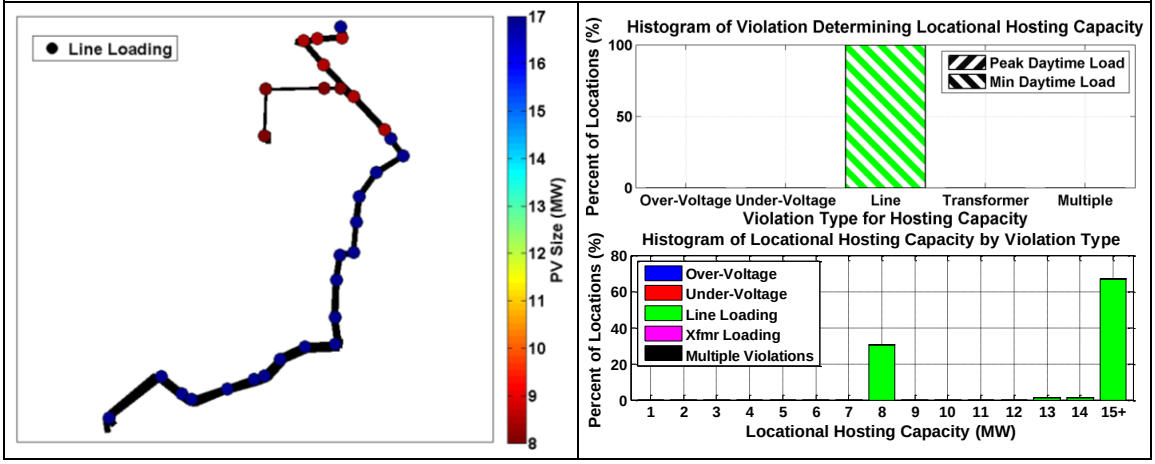
GN7



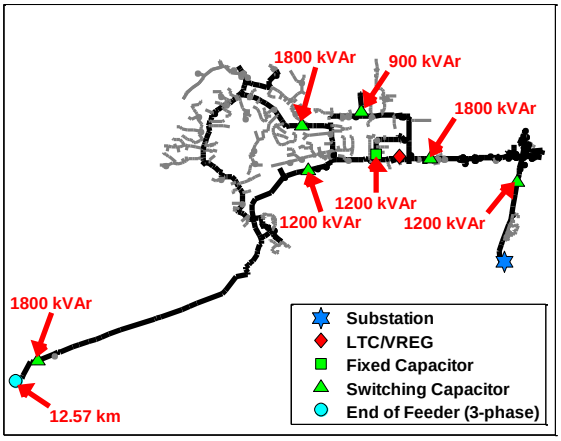
PV Impact Signature



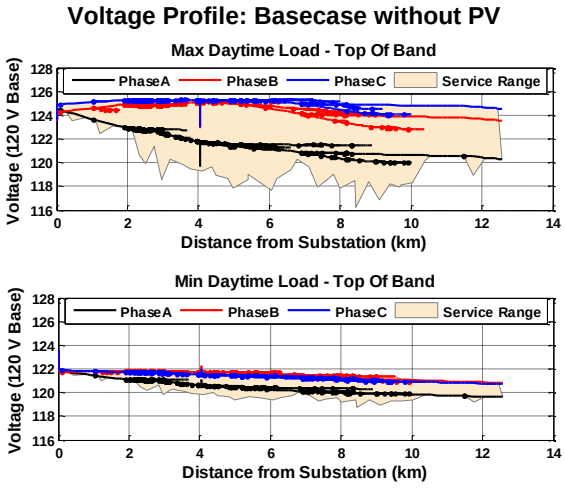
Locational Hosting Capacity



QL1

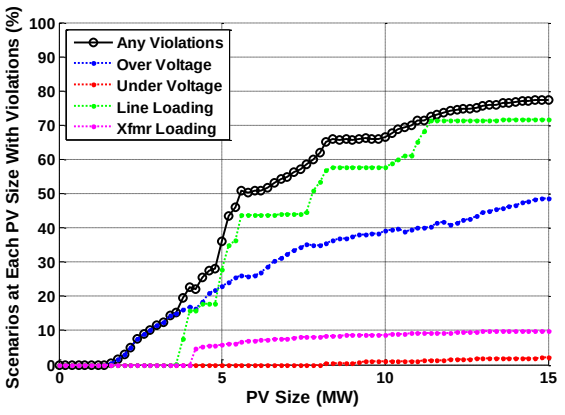


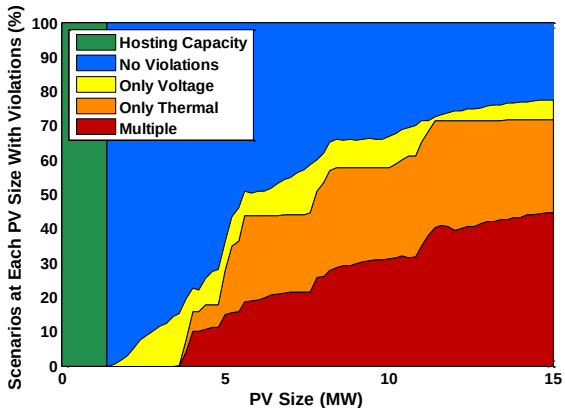
20.78 kV, 18.63 MW peak load
Max daytime load = 16.91 MW (91%)
Min daytime load = 4.96 MW (27%)



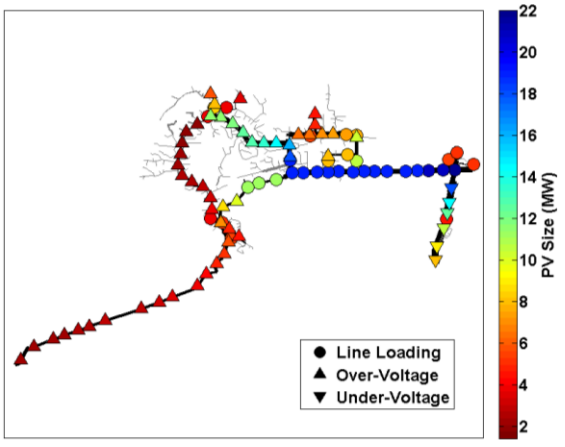
Bottom of Band bus voltages average 1.28 V lower

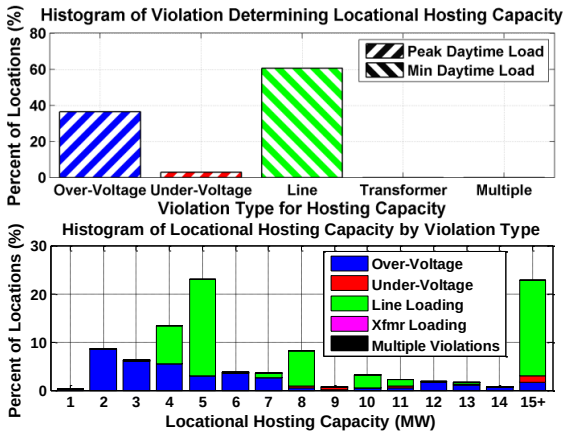
PV Impact Signature



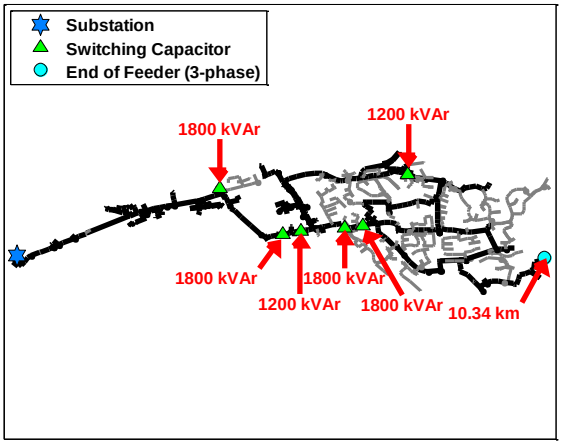


Locational Hosting Capacity

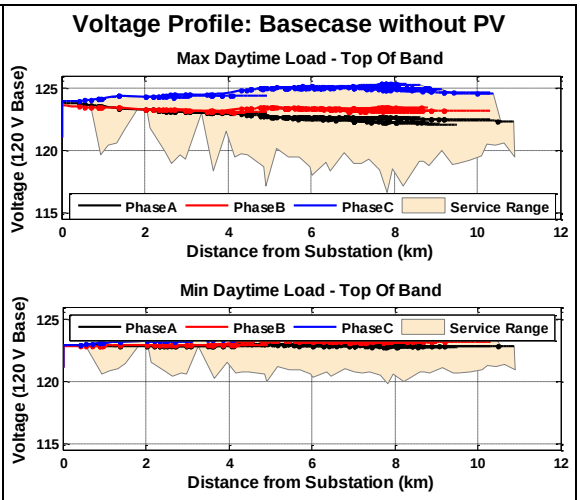




QN1

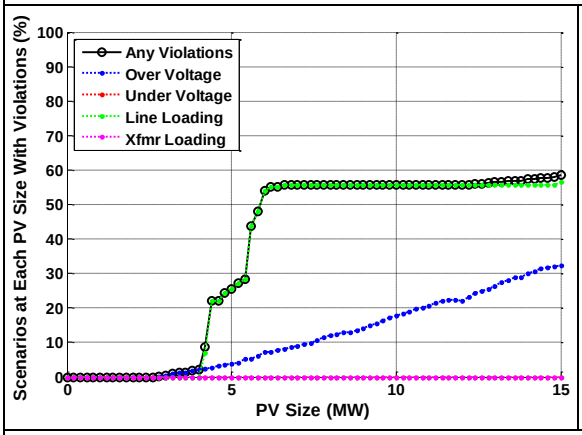


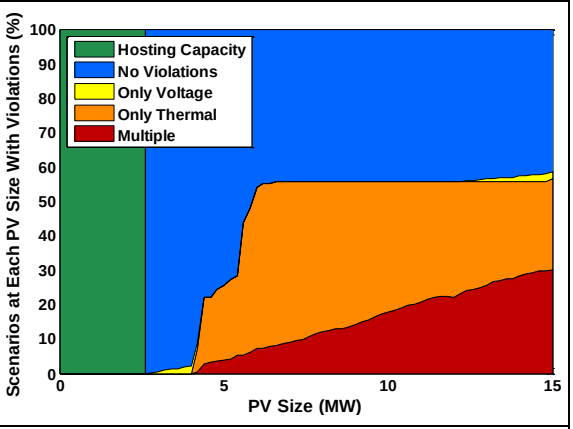
20.78 kV, 16.71 MW peak load
Max daytime load = 16.08 MW (96%)
Min daytime load = 6.23 MW (37%)



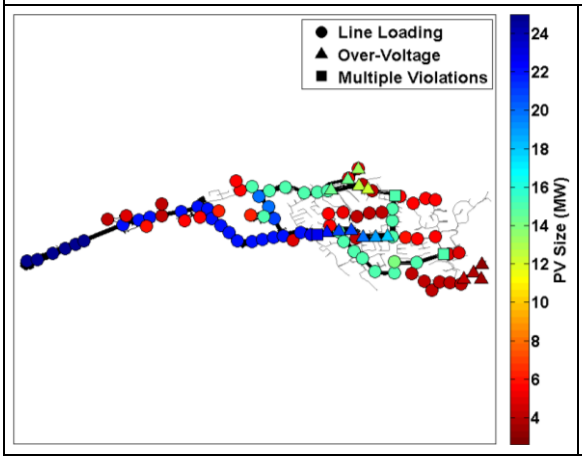
Bottom of Band bus voltages average 1.46 V lower

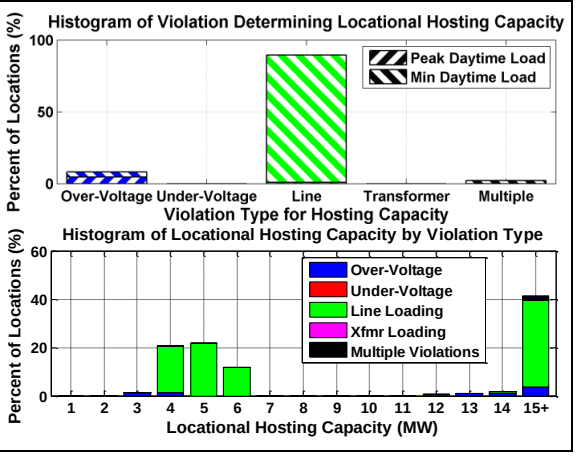
PV Impact Signature



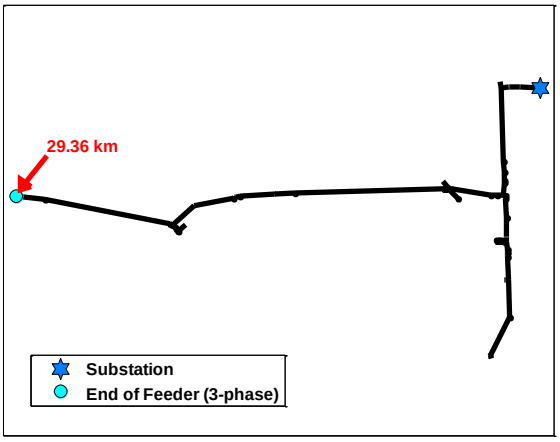


Locational Hosting Capacity



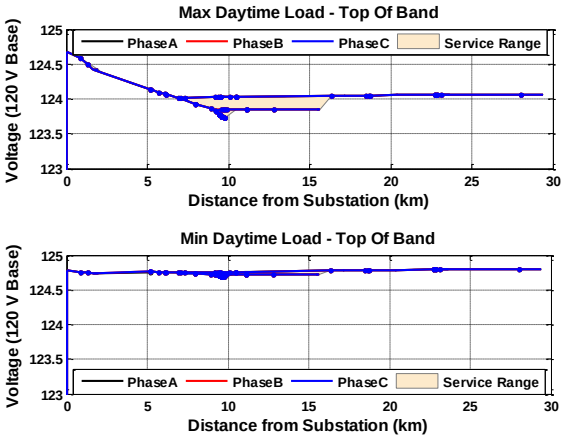


CH1



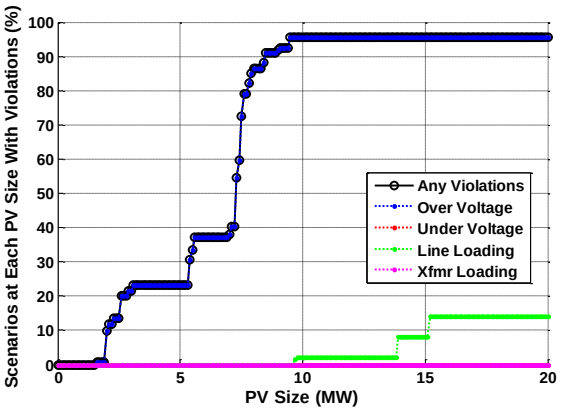
33 kV, 16.48 MW peak load
Max daytime load = 15.84 MW (96%)
Min daytime load = 5.11 MW (31%)

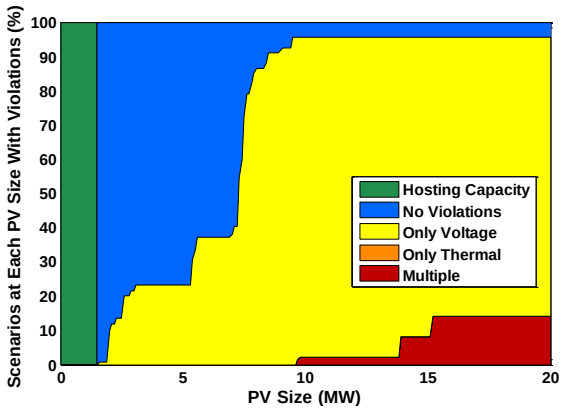
Voltage Profile: Basecase without PV



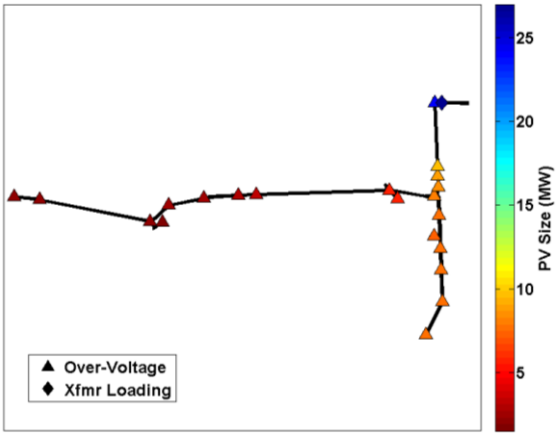
Bottom of Band bus voltages average 0.99 V lower

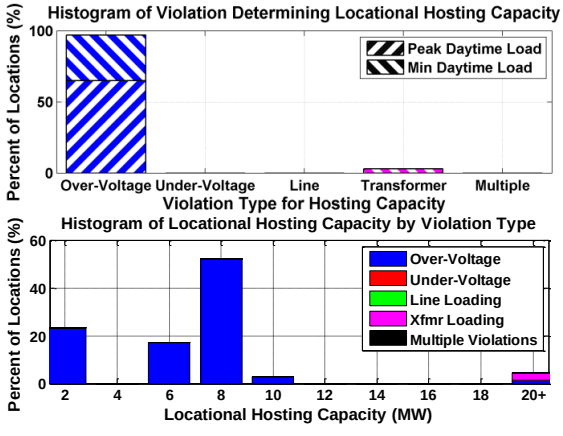
PV Impact Signature



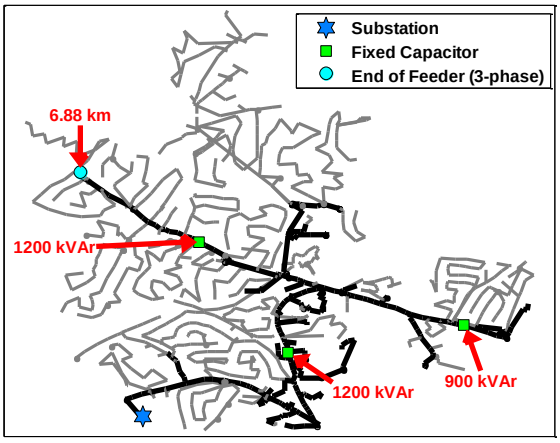


Locational Hosting Capacity

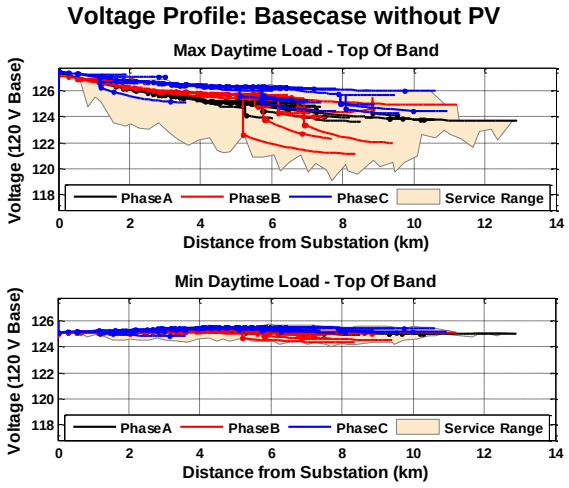




Ckt24

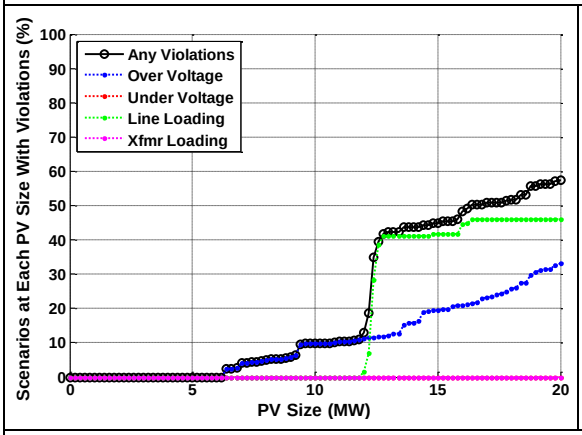


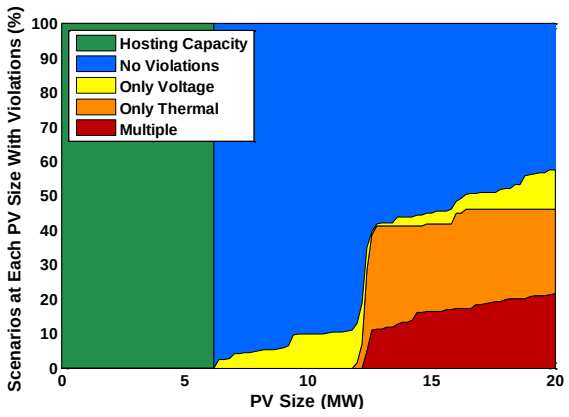
34.5 / 13.2 kV (34.5 kV analyzed), 28.45 MW peak load
Max daytime load = 28.45 MW (100%)
Min daytime load = 6.06 MW (21%)



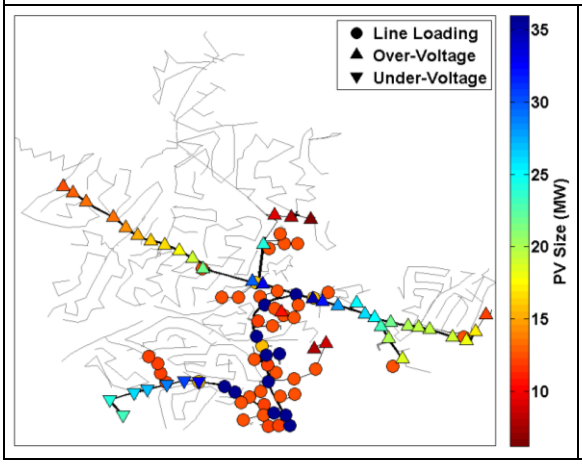
Bottom of Band bus voltages average 2.94V lower

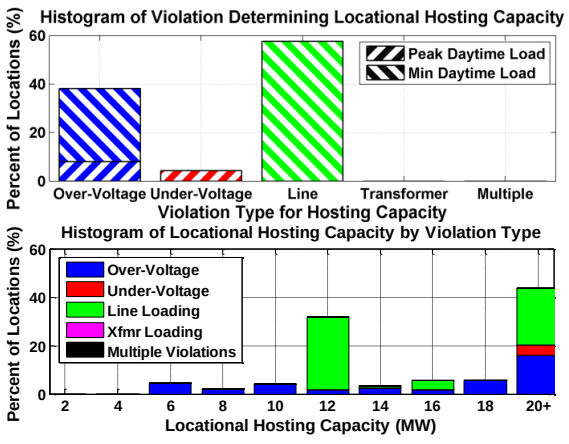
PV Impact Signature





Locational Hosting Capacity





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